Peng Wu

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RESEARCH INTERESTS

- Experimental study on nanoscale transistors based on two-dimensional (2D) materials for beyond-CMOS applications, such as hardware security and in-memory computing
- Low-power steep-slope transistors, including TFET and cold-source/Dirac-source FET
- Semiconductor physics and electron transport in nanoscale transistors

EDUCATION

Purdue University Aug. 2015 - Oct. 2021
PhD in Electrical and Computer Engineering, GPA: 4.0/4.0
Thesis: Two-Dimensional Nano-Transistors for Steep-Slope Devices and Hardware Security

Tsinghua University Aug. 2011 - Jul. 2015
Bachelor in Microelectronics, GPA: 92.9/100

RESEARCH EXPERIENCE

Postdoctoral Associate Nov. 2021 - Present
MIT, Research Laboratory of Electronics **Advisor: Prof. Jing Kong**

- Investigated steep-slope cold-source FET based on 2D materials.
- Developed 2D ferroelectric FET for in-memory computing.
- Studied contact strategy to 2D materials for PMOS transistors.

Graduate Research Assistant Aug. 2015 - Oct. 2021
Purdue University, School of ECE **Advisor: Prof. Joerg Appenzeller**

- Performed experimental study on novel transistor applications based on 2D materials.
- Developed secure circuits based on 2D reconfigurable FETs with tunable polarity (first-author paper published in *Nature Electronics*).
- Demonstrated complementary TFET based on 2D material black phosphorus (first-author paper published in *ACS Nano*).
- Helped write proposals & secure research funding from Intel, Semiconductor Research Corporation (SRC), Applied Research Institute (ARI), etc.

Undergraduate Researcher Sep. 2014 - Jul. 2015
Tsinghua University, Institute of Microelectronics **Advisors: Profs. Zhiping Yu & Jinyu Zhang**

- Studied modeling and TCAD simulation of double-gate TFET.

Undergraduate Exchange Student Researcher Apr. 2014 - Sep. 2014
HKUST, Department of ECE **Advisor: Prof. Mansun Chan**

- Studied modeling of NBTI in SiON gate-dielectric MOSFET under DC and AC biases.

AWARDS AND RECOGNITIONS

- Runner-up, Science Communication Shark Tank Competition at Birck Nanotechnology Center (2020)
- Third Place Poster Prize, 3rd Annual Microelectronics Integrity Meeting Poster Contest (2018)
- Best Poster Award, SRC LEAST Center Annual Review (2017)
- Outstanding Graduate (Top 10%), Tsinghua University (2015)

· Scholarship for Academic/Comprehensive Excellence, Tsinghua University (2012-2014)

PROFESSIONAL SERVICE

Membership

· IEEE Member

Reviewer

· *Nature*, *Nature Electronics*, *Nature Communications*, *Advanced Materials*, *Nano Letters*, *IEEE Transactions on Electron Devices* (**Golden Reviewer**, 2022), *IEEE Electron Device Letters* (**Golden Reviewer**, 2020-2023), *ACS Applied Nano Materials*, *ACS Applied Electronic Materials*, *Journal of Computational Electronics*, *physica status solidi (a)*.

Volunteering activities

MIT.nano tour guide:

· Guided tours to 20+ people to the state-of-the-art nanofabrication and characterization facilities at MIT.nano.

JOURNAL PUBLICATIONS

In preparation/Submitted/Accepted

3. **Peng Wu**, Steven A. Vitale, Kevin Tibbetts, Jing Kong, "Quantitative Evaluation of Rethermalization in Cold-Source FET using Boltzmann Transport Equation," *in preparation*.
2. **Peng Wu**[†], Jun Cai[†], Mengyuan Li, Xiaobo Sharon Hu, Jing Kong, "2D ferroelectric multi-bit content-addressable memory for efficient in-memory computing," *in preparation*.
1. **Peng Wu**, Jun Cai, Joerg Appenzeller, "Cold-source FET," accepted by ***APL Materials*** (Invited mini-review).

Journal articles

21. **Peng Wu**, Tianyi Zhang, Jiadi Zhu, Tomás Palacios, Jing Kong, "2D materials for logic device scaling," ***Nature Materials*** **23**, 23-25 (2024) (Invited mini-review).
20. **Peng Wu**, "Mobility overestimation in molybdenum disulfide transistors due to invasive voltage probes," ***Nature Electronics*** **6**, 836–838 (2023) (Matters Arising).
19. Jun Cai, Zheng Sun, **Peng Wu**, Rahul Tripathi, Hao-Yu Lan, Jing Kong, Zhihong Chen, Joerg Appenzeller, "High-Performance Complementary Circuits from Two-Dimensional $MoTe_2$," ***Nano Letters*** **23**, 10939–10945 (2023).
18. Tianyi Zhang, Jiangtao Wang, **Peng Wu**, Ang-Yu Lu, Jing Kong, "Vapour-phase deposition of two-dimensional layered chalcogenides," ***Nature Reviews Materials*** **8**, 799–821 (2023) (Invited review).
17. Zheng Sun, Chin-Sheng Pang, **Peng Wu**, Terry Y.T. Hung, Ming-Yang Li, San Lin Liew, Chao-Ching Cheng, Han Wang, H.-S. Philip Wong, Lain-Jong Li, Iuliana Radu, Zhihong Chen, Joerg Appenzeller, "Statistical Assessment of High-Performance Scaled Double-Gate Transistors from Monolayer WS_2," ***ACS Nano*** **16**, 14942–14950 (2022).
16. Mengyuan Li, **Peng Wu**, Bo Zhou, Xiaobo Sharon Hu, Joerg Appenzeller, "Cross-Coupled Gated Tunneling Diodes With Unprecedented PVCRs Enabling Compact SRAM Design—Part II: SRAM Circuit," ***IEEE Transactions on Electron Devices*** **69** (11), 6078-6084 (2022).
15. **Peng Wu**, Mengyuan Li, Bo Zhou, Xiaobo Sharon Hu, Joerg Appenzeller, "Cross-Coupled Gated Tunneling Diodes With Unprecedented PVCRs Enabling Compact SRAM Design—Part I: Device Concept," ***IEEE Transactions on Electron Devices*** **69** (11), 6078-6084 (2022).
14. **Peng Wu**, Joerg Appenzeller, "Explaining Steep-Slope Switching in Carbon Nanotube Dirac-Source Field-Effect Transistors," ***IEEE Transactions on Electron Devices*** **69** (9), 5270-5275 (2022).
13. **Peng Wu**, Joerg Appenzeller, "Design Considerations for 2-D Dirac-Source FETs—Part II: Nonidealities and Benchmarking," ***IEEE Transactions on Electron Devices*** **69** (8), 4681–4685 (2022).

[†]equal contribution

12. **Peng Wu**, Joerg Appenzeller, "Design Considerations for 2-D Dirac-Source FETs—Part I: Basic Operation and Device Parameters," ***IEEE Transactions on Electron Devices*** **69** (8), 4674–4680 (2022).

11. Chin-Sheng Pang, **Peng Wu**, Joerg Appenzeller, Zhihong Chen, "Thickness-Dependent Study of High-Performance WS_2-FETs With Ultrascaled Channel Lengths," ***IEEE Transactions on Electron Devices*** **68** (4), 2123-2129 (2021).

10. Chin-Cheng Chiang, Vaibhav Ostwal, **Peng Wu**, Chin-Sheng Pang, Feng Zhang, Zhihong Chen, Joerg Appenzeller, "Memory Applications from 2D Materials," ***Applied Physics Reviews*** **8**, 021306 (2021).

9. Chin-Sheng Pang, Ruiping Zhou, Xiangkai Liu, **Peng Wu**, Terry Y. T. Hung, Shiqi Guo, Mona E. Zaghloul, Sergiy Krylyuk, Albert V. Davydov, Joerg Appenzeller, Zhihong Chen, "Mobility Extraction in 2D Transition Metal Dichalcogenide Devices—Avoiding Contact Resistance Implicated Overestimation," ***Small*** **17**, 2100940 (2021).

8. **Peng Wu**, Joerg Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor Without a Ferroelectric Component," ***ACS Nano*** **15**, 5158– 5164 (2021).

7. **Peng Wu**, Dayane Reis, Xiaobo Sharon Hu, Joerg Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," ***Nature Electronics*** **4**, 45-53 (2021).
(Featured on Purdue News, ArsTechnica)

6. **Peng Wu**, Joerg Appenzeller, "Toward CMOS like devices from two-dimensional channel materials," ***APL Materials*** **7**, 100701 (2019) *(Editor's Pick).*

5. **Peng Wu**, Joerg Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor With Record High ON-Currents," ***IEEE Electron Device Letters*** **40**, 981-984 (2019).

4. **Peng Wu**, Tarek Ameen, Huairuo Zhang, Leonid A. Bendersky, Hesameddin Ilatikhameneh, Gerhard Klimeck, Rajib Rahman, Albert V. Davydov, Joerg Appenzeller, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," ***ACS Nano*** **13**, 377-385 (2018).

3. Bernhard Stampfer, Feng Zhang, Yury Yuryevich Illarionov, Theresia Knobloch, **Peng Wu**, Michael Waltl, Alexander Grill, Joerg Appenzeller, Tibor Grasser, "Characterization of Single Defects in Ultrascaled MoS_2 Field-Effect Transistors," ***ACS Nano*** **12**, 5368-5375 (2018).

2. Abhijith Prakash, Hesameddin Ilatikhameneh, **Peng Wu**, Joerg Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," ***Scientific Reports*** **7**, 12596 (2017).

1. Guo Zhang, Jinyu Zhang, Zhan Liu, **Peng Wu**, Huaqiang Wu, He Qian, Yan Wang, Zhiyong Zhang, Zhiping Yu, "Geometry Optimization of Planar Hall Devices Under Voltage Biasing," ***IEEE Transactions on Electron Devices*** **61** (12), 4216-4223 (2014).

CONFERENCE PUBLICATIONS & PRESENTATIONS

8. Jun Cai, **Peng Wu**, Rahul Tripathi, Zhihong Chen, Jing Kong and Joerg Appenzeller, "Ultra-compact ternary content-addressable memory cell based on single ambipolar two-dimensional floating-gate transistor," *81st Device Research Conference (DRC)*, 2023 (Oral presentation).

7. Chin-Sheng Pang, **Peng Wu**, Joerg Appenzeller, Zhihong Chen, "Sub-1nm EOT WS_2-FET with $I_{DS} > 600$ μA/μm at $V_{DS} = 1$V and SS < 70mV/dec at $L_G = 40$nm," *66th IEEE International Electron Devices Meeting (IEDM)*, 2020 (Oral presentation).

6. Theresia Knobloch, Jakob Michl, Dominic Waldhör, Yury Illarionov, Bernhard Stampfer, Alexander Grill, Ruiping Zhou, **Peng Wu**, Michael Waltl, Joerg Appenzeller, Tibor Grasser, "Analysis of single electron traps in nano-scaled MoS_2 FETs at cryogenic temperatures," *78th Device Research Conference (DRC)*, 2020 (Oral presentation).

5. **Peng Wu**, Ruiping Zhou, Chin-Sheng Pang, Xiangkai Liu, Zhihong Chen, Joerg Appenzeller, "Contact Resistance Model for WSe_2 Schottky-Barrier FET," *78th Device Research Conference (DRC)*, 2020 (Oral presentation).

4. **Peng Wu**, Joerg Appenzeller, "High Performance Complementary Black Phosphorus FETs and Inverter Circuits Operating at Record-Low V_{DD} down to 0.2V," *76th Device Research Conference (DRC)*, 2018 (Oral presentation).

3. **Peng Wu**, Abhijith Prakash, Joerg Appenzeller, "First demonstration of band-to-band tunneling in black phosphorus," *75th Device Research Conference (DRC)*, 2017 (Oral presentation).

2. **Peng Wu**, Jinyu Zhang, Li Zhang, Zhiping Yu, "Channel-Potential Based Compact Model of Double-Gate Tunneling FETs Considering Channel-Length Scaling," *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2015 (Oral presentation).

1. **Peng Wu**, Chenyue Ma, Lining Zhang, Xinnan Lin, Mansun Chan, "Investigation of Nitrogen Enhanced NBTI Effect Using the Universal Prediction Model," *IEEE International Reliability Physics Symposium (IRPS)*, 2015 (Poster presentation).

PATENT APPLICATION

1. **Peng Wu**, Joerg Appenzeller, "CROSS-COUPLED GATED TUNNEL DIODE (XTD) DEVICE WITH INCREASED PEAK-TO-VALLEY CURRENT RATIO (PVCR)," *U.S. Patent*, Application No. 17/690,417, filed March 9, 2022.

REFERENCES

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