High-Speed Analog-to-Digital Converter Survey

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Every year, higher and higher sampling rates as well as lower and lower power dissipations are reported in the literature. The table in Figure 1 lists published results for nineteen high-speed, low-resolution A/D converters (mostly six to eight bits), along with a few commercial parts, representing a wide variety of fabrication technologies. In the following sections, these reported specifications are analyzed and compared.

1 Quantization Energy Figure of Merit

The analog program committee of the IEEE International Solid-State Circuits Conference suggested a figure of merit for A/D converters that takes into account power dissipation, resolution, and sampling rate [1]. It has units of energy, and represents the energy used per conversion step

$$E = \frac{P}{2^N F_S}$$

where P is the power dissipation, N is the stated number of bits, and F_S is the sampling rate. This quantity is nearly the inverse of a similar figure of merit suggested earlier by Robert Walden [2, 3] that uses the *effective* number of bits (ENOB), B, instead of the stated number of bits

$$F = \frac{2^B F_S}{P}$$

Walden's figure of merit F correctly includes the performance limitation of signal-to-noise-and-distortion ratio (SNDR), but still produces optimistic results for some A/D converters[1]. In most applications, A/D converters are expected to faithfully convert all input-signal frequencies below the Nyquist frequency (one half of the sampling rate F_S), but many A/D converters exhibit severe degradation of SNDR at frequencies well below the Nyquist frequency. For this reason, the literature has recently started using the effective resolution bandwidth (ERBW) instead of the sampling rate in the equation for the figure of merit [4, 5]. This figure of merit is known as the "quantization energy"

$$E_Q = \frac{P}{2^B (2F_{BW})}$$

where P is the power dissipation, B is the high-frequency ENOB (calculated from SNDR), and F_{BW} is either the effective resolution bandwidth or the Nyquist frequency, which ever is less.

[1] Hopeless pedants, like this author [6], also complain about its nonsensical units of "inverse joules."

Pub Year	F_S MS/s	stated bits	ENOB bits	ERBW MHz	Power mW	E_Q pJ	Pub Ref
CMOS Flash Topologies							
1998	200	6	5.0	100	380	59.4	[7]
1998	350	6	5.8	87	225	23.2	[8]
1998	400	6	5.0	100	190	29.7	[9]
1998	400	6	4.7	100	200	38.5	[10]
1999	500	6	5.3	250	400	20.3	[11]
1999	500	6	4.7	50	330	127	[12]
1999	500	6	5.3	180	225	15.9	[13]
2000	600	6	4.7	150	193	24.8	[14]
2000	700	6	5.5	136	187	15.2	[15]
2000	800	6	5.0	200	400	31.3	[16]
2001	1100	6	5.3	450	300	8.5	[4]
2001	1300	6	5.0	650	545	13.1	[17]
2002	1600	6	5.2	600	328	7.4	[5]
Bipolar Processes (including Si, GaAs, InP, etc)							
1995	2000	8	6.5	1000	5300	29.3	[18]
1995	4000	6	5.1	1800	5700	46.2	[3, 19]
1996	8000	3	2.4	4000	3500	82.9	[20]
1999	500	8	7.2	250	950	12.9	[21]
Interleaved Topologies							
1997	8000	8	5.3	2000	13500	85.7	[22]
2002	4000	8	6.5	900	2400	14.7	[23]
Commercial Parts							
1995	1000	8	5.5	500	5500	122	[24]
1998	2000	8	5.9	500	5000	83.7	[25]
2001	1500	8	7.5	750	5300	19.5	[26]

Figure 1: Table of nineteen high-speed analog-to-digital converter specifications gathered from the literature, along with commercial parts from Fairchild, Rockwell, and Maxim.

2 High Speed

High-speed analog-to-digital converters are used in radar signal receivers, digital sampling oscilloscopes, read channels for magnetic storage systems, and local-area-network interfaces. Figure 2 shows the steady increase in effective resolution bandwidth with time. The average speed of high-speed A/D converters has increased by a factor of ten over the past five years.

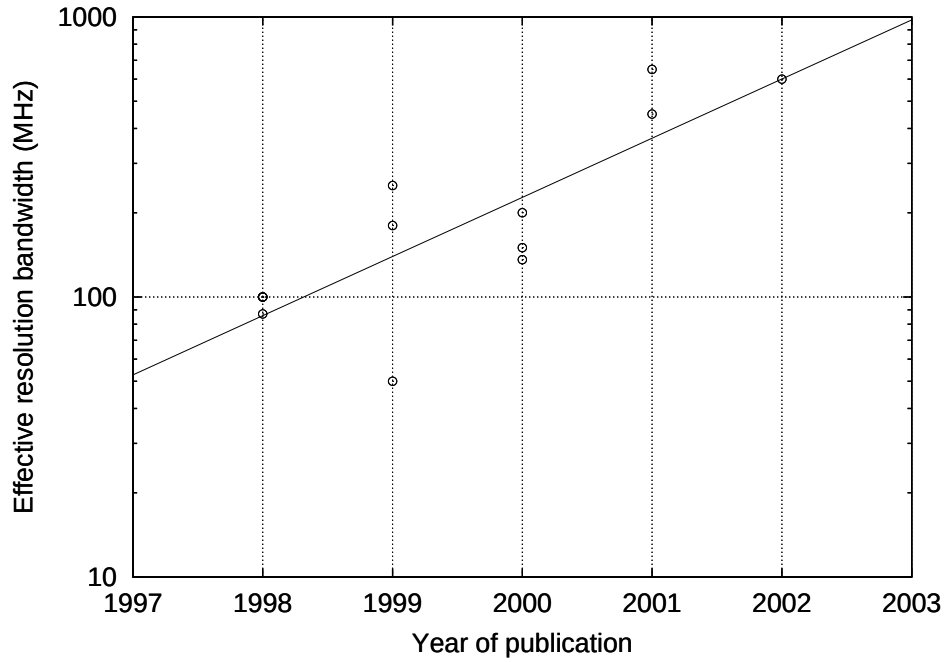

Figure 2: Published CMOS flash A/D converters: effective resolution bandwidth versus year of publication. The best-fit line shows a factor of ten increase in ERBW over five years.

3 Low Power

In this era of wireless communications, portable high-speed test equipment, and networked laptop computers, the motivation for low-power electronics is clear. Reducing the power requirements of existing components extends the battery life of portable devices, or allows additional functionality to be incorporated on the same power budget. Alternatively, battery size (a significant, often dominant, contribution to the size and weight of portable devices) can be reduced by decreasing the power consumption while maintaining feature set and battery life.

The total power consumption of massively-parallel systems, such as phased-array radar systems, is also a concern, if for no other reason than the attendant cooling issues.

Figure 3 shows a minimum quantization energy of about 10 picojoules/conversion-step for a wide range of bandwidths, with a sharp rise above one gigahertz. However, Figure 4 shows that much of this progress in efficiency has occurred recently, with the lowest reported quantization energy decreasing yearly. Unfortunately, this data shows slow progress, with only a factor of ten improvement over nine years.

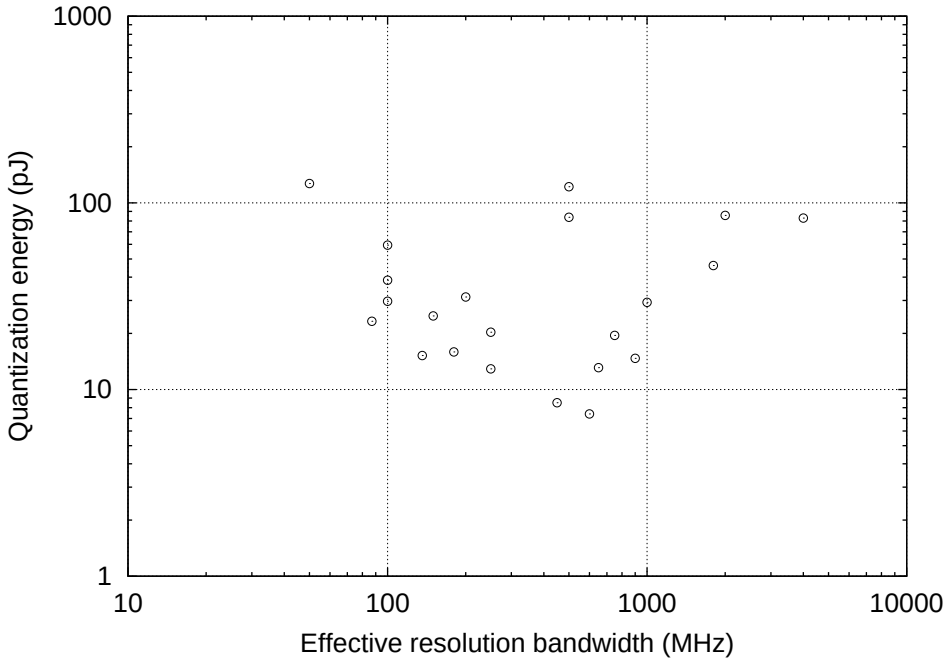

Figure 3: All high-speed flash A/D converters: quantization energy versus effective resolution bandwidth.

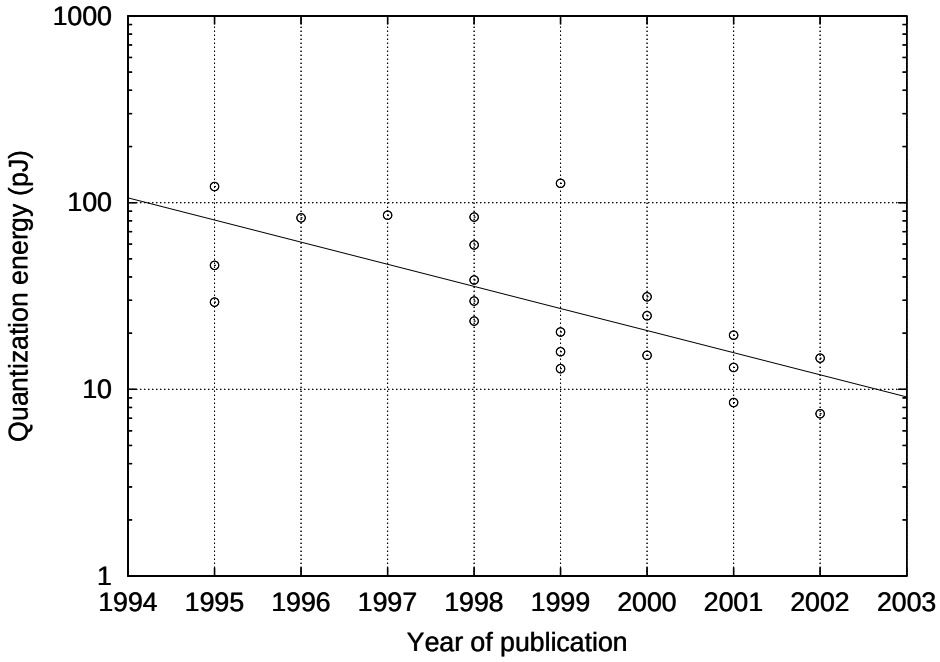

Figure 4: All high-speed flash A/D converters: quantization energy versus year of publication. The best-fit line shows a factor of ten improvement in quantization energy over nine years.

4 Absolute Minimum Power

The absolute minimum power for an analog-to-digital converter can be calculated from first principles [27, 28]. Assuming that the voltage to be converted is sampled and stored on a single capacitor, C, the minimum thermal noise is

$$V_{\mathrm{ntc}}^2 = \frac{kT}{C}$$

If this capacitor is charged and discharged during every conversion cycle, the maximum power dissipated is

$$P = CV_{FS}^2 F_S$$

where V_{FS} is the full-scale voltage of the A/D converter and F_S is the sampling rate. The quantization noise for this A/D converter is

$$V_{\mathrm{nq}}^2 = \frac{V_{\mathrm{LSB}}^2}{12} = \frac{V_{FS}^2}{2^{2N}12}$$

Limiting the thermal-noise power to be less than one quarter of the quantization-noise power, the total signal-to-noise ratio of the A/D converter will be degraded by less than 1 dB (since 1 dB corresponds to a factor of 1.25 in power units)

$$\frac{kT}{C} < \frac{1}{4}\left(\frac{V_{FS}^2}{2^{2N}12}\right)$$

Solving this inequality for the expression $V_{FS}^2 C$

$$V_{FS}^2 C > 48kT\,2^{2N}$$

and substituting this quantity into the above expression for power gives the final result

$$P > 48kT\,2^{2N} F_S$$

This expression implies an absolute lower bound on the quantization energy E_Q for an A/D converter of a given resolution N at any speed

$$E_Q = \frac{P}{2^N F_S} > \frac{48kT\,2^{2N} F_S}{2^N F_S} = 48kT\,2^N$$

for a six-bit A/D converter at room temperature (such as most of the A/D converters listed in Figure 1), this limit is

$$E_Q > 1.3 \times 10^{-17} J$$

which is more than five orders of magnitude below the best A/D converter in Figure 4.

5 Aperture Jitter

A limitation in the performance of state-of-the-art A/D converters has been observed and commented on by Robert Walden [3]. Aperture jitter is the the sample-to-sample variation in the instant of conversion. There is an rms voltage error caused by rms aperture jitter (measured in picoseconds), and it decreases the overall signal-to-noise ratio.

Since the aperture-time variations are random, these voltage errors behave like a random noise source. The signal-to-jitter-noise ratio can be expressed as

$$\text{SJNR} = 20 \log \left(\frac{1}{2\pi t_a F_S} \right)$$

The graph in Figure 5 shows the effective number of bits versus sampling rate for the A/D converters listed in Figure 1. No A/D converter exhibits an aperture uncertainty better than 0.4 ps. Walden observes that this situation has not improved much over time, and will not without significant research and development.

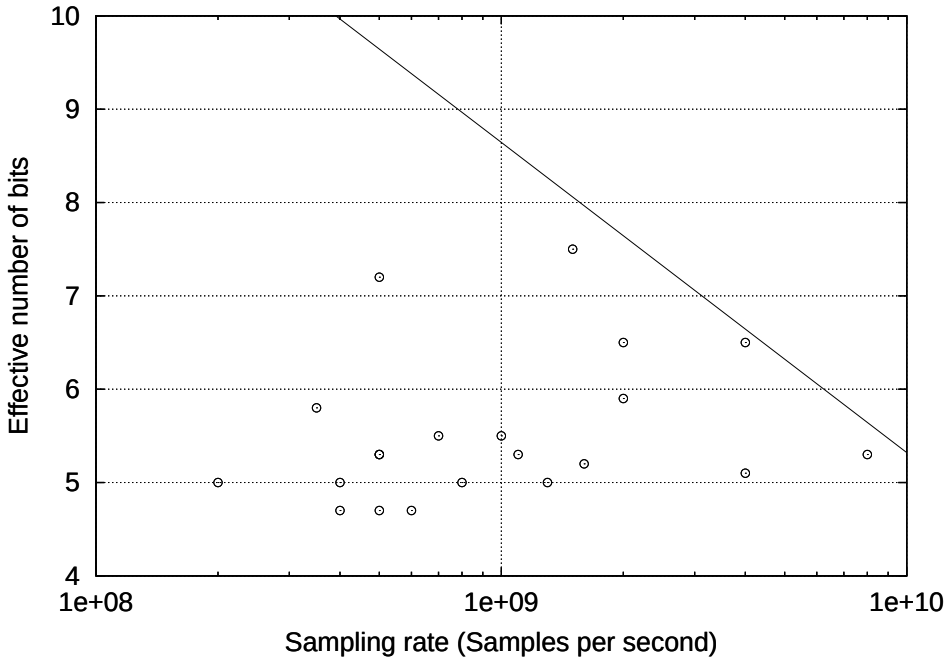

Figure 5: All high-speed flash A/D converters: effective number of bits versus sampling rate. The line corresponds to the limitation imposed by an rms aperture jitter of 0.4 ps.

6 Additional Power Consumption

Clearly, thermal noise is not the only limiting factor, and the simply-derived lower bound on power may never be approached. The development in Section 4 considers only the power consumption of an ideal sample-and-hold. It completely ignores the power consumption of active circuitry in the A/D converter for analog amplification or digital encoding. The power required to drive parasitic capacitances was also ignored. Considering these real-world requirements, several other limitations on performance can be calculated.

6.1 Transistor Matching

Random voltage offsets in the comparators cause a limitation to accuracy that can only be overcome with improved transistor matching. Offset reduction through transistor matching increases power consumption. Transistor matching can be improved by increasing device size (which increases parasitic capacitances), by introducing calibration or error-correcting techniques (which consume additional power), or by introducing auto-zero cycles (which decrease speed). The additional power required to overcome the effects of transistor mismatch in high-speed CMOS systems is two orders of magnitude higher than the limit imposed by thermal noise [29, 30].

Reported data shows that transistor matching improves with decreasing gate-oxide thickness [30], thus for the same transistor area higher accuracy and speed, or lower power consumption, should be achievable in a technology with smaller feature sizes. However, lower supply voltages adversely affect the signal-to-noise ratio and decrease the potential improvements [31].

6.2 Device Parasitics

Scaled technologies with smaller feature sizes often have larger parasitics, since the increased doping increases the values of the depletion capacitances that form around the junctions. These parasitics directly affect performance. In particular, gate-overlap capacitances and drain-to-bulk depletion-layer capacitances have been shown to have increasing influence in scaled processes [32]. It is possible that power consumption will actually need to increase to maintain accuracy and speed in the face of shrinking feature sizes [33].

6.3 Calibration

Calibration of A/D converters generally increases power consumption and decreases speed. Comparable digital and analog calibration techniques [34, 35], designed for similar performance improvements, significantly increase power consumption.

7 Conclusions

Aperture jitter, transistor matching, and increasing drain-bulk capacitance remain major problems in the development of high-speed, low-power A/D converters. In spite of these difficulties, steady progress in speed and power has been made in recent years, as shown in Figures 2 and 4.

Following these trends, a six-bit A/D converter with a 10-GHz effective resolution bandwidth will be available in five to six years, but with a projected quantization energy of $E_Q = 3$ pJ, it will carry a power consumption of four watts.

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