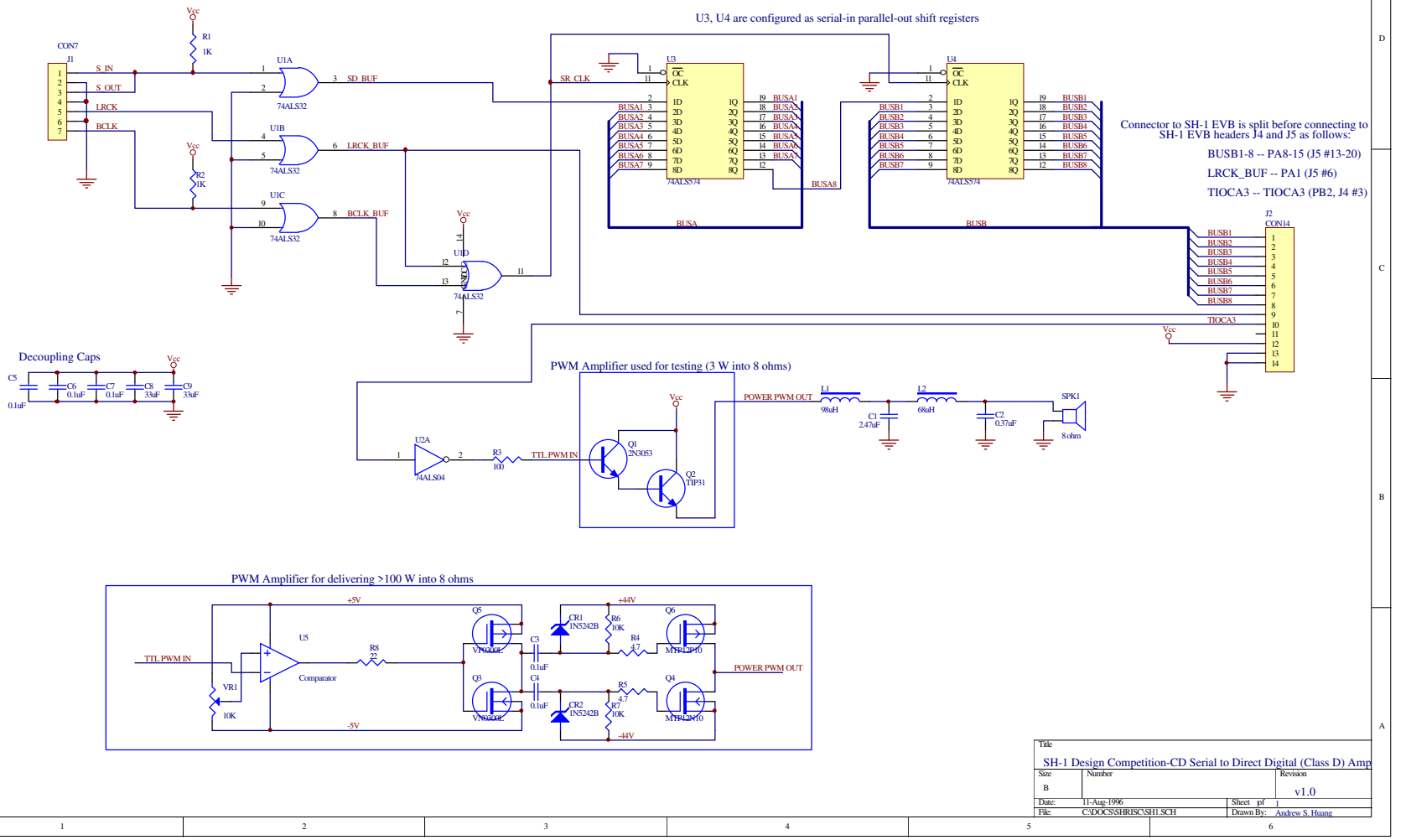
Data from CD player has 3V CMOS logic levels
U3, U4 are configured as serial-in parallel-out shift registers
Connector to SH-1 EVB is split before connecting to SH-1 EVB headers J4 and J5 as follows:
BUSB1-8 -- PA8-15 (J5 #13-20)
LRCK_BUF -- PA1 (J5 #6)
TIOCA3 -- TIOCA3 (PB2, J4 #3)
Decoupling Caps
PWM Amplifier used for testing (3 W into 8 ohms)
PWM Amplifier for delivering >100 W into 8 ohms
SH-1 Design Competition-CD Serial to Direct Digital (Class D) Amp
Size B
Number
Revision v1.0
Date: 11-Aug-1996
Sheet pf 1
File: C:\DOCS\SHRISC\SH1.SCH
Drawn By: Andrew S. Huang