All-Optical Processing for Ultrafast Data Networks Using Semiconductor Optical Amplifiers

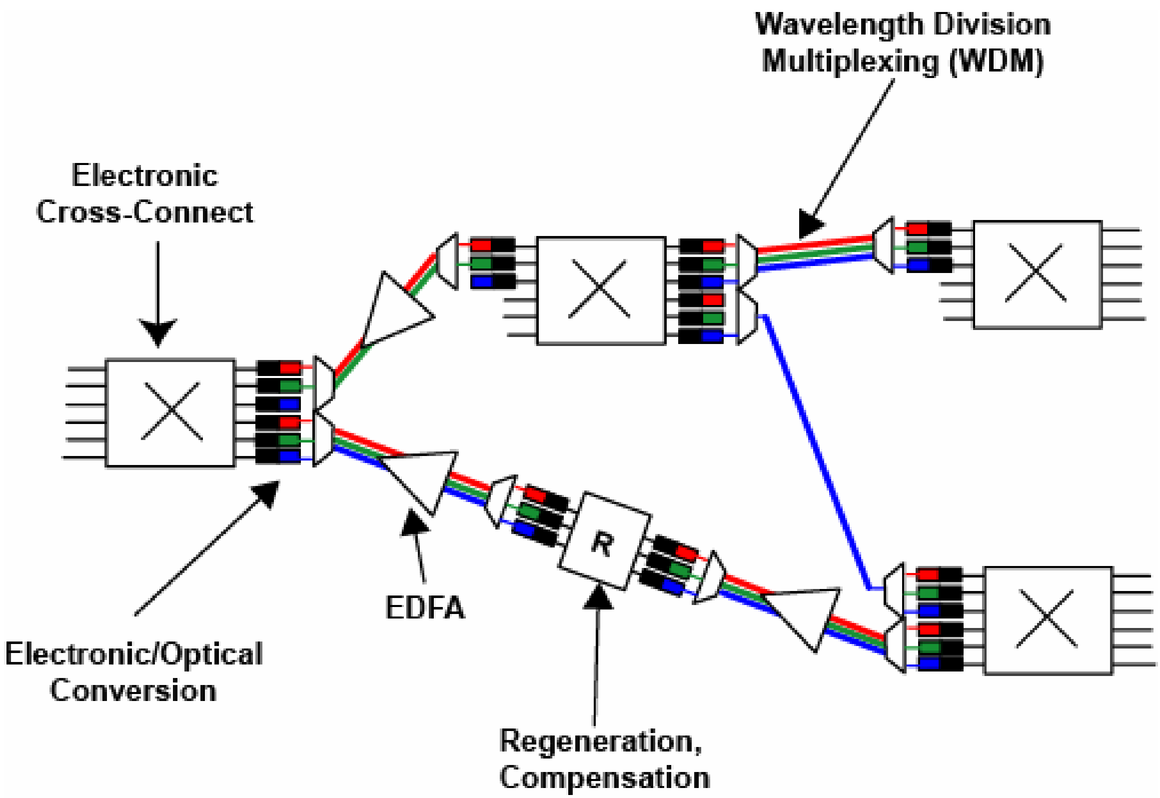
Jade P. Wang

Ph.D. Thesis Defense

Thesis Committee: Professor Erich P. Ippen, Dr. Scott A. Hamilton, Professor Rajeev J. Ram

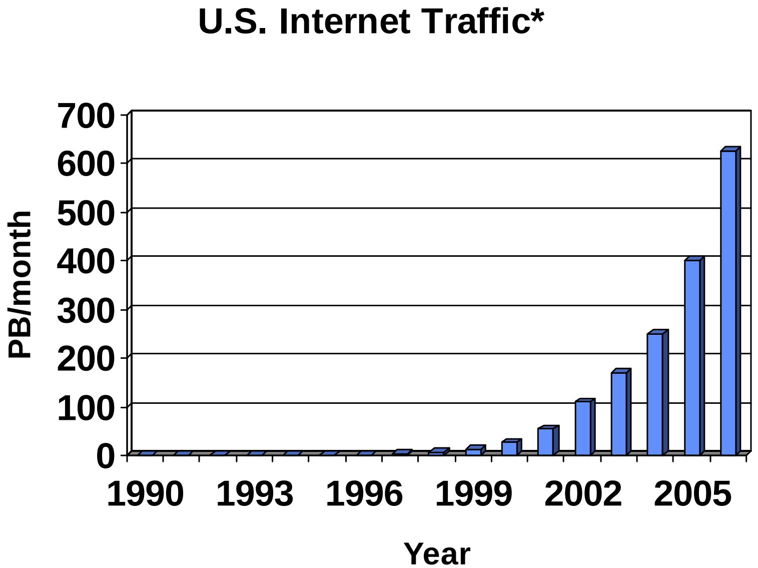
Today's Data Networks

- **Transmission over optical fiber**
  - **Wavelength division multiplexing (WDM) : multiple wavelength channels per fiber**
  - **Erbium-doped fiber amplifiers (EDFAs): multi-wavelength amplification**
  - **Electronic regenerators with O/E/O conversion & demultiplexing**
- **Electronic routers with O/E/O conversion & demultiplexing**

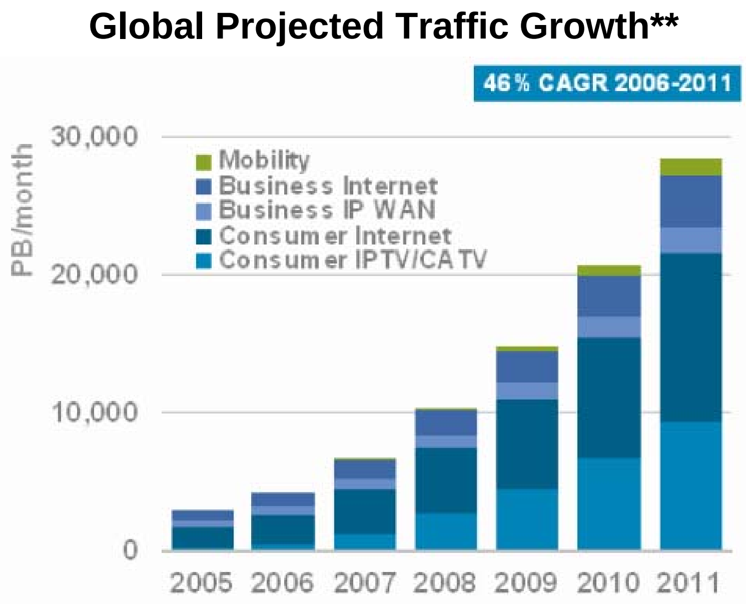


- **WDM: 80+ channels, 10-40 Gb/s per channel**
- **EDFA: 60-80 km spacing**
- **Regenerator: Every 2-3 spans (120-240 km)**
- **Routers: 100+ ports with 1+ Tb/s throughput**

Increasing Demand for Capacity



*Odlyzko et al., "Internet Growth Trends and Moore's Law"
http://www.dtc.umn.edu/mints/igrowth.html



**Cisco, "The Exabyte Era", 2008

- **Steady growth estimated at 50%-100% / year**
- **Increasing video traffic (YouTube, IPTV, Video on Demand)**
- **High-end users: storage networks, data centers, grid computing, scientific processing**
- **Growing number of internet users around the world**

→ **Increasing channel bit rates and number of channels**

Outline

- Motivation/Background
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
- Performance optimization of optical logic gates
- Regeneration
- Future SOA-MZI gates
- Conclusion

Outline

- **Motivation/Background: Why all-optical processing?**
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
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Optical Signal Processing

- **Ultrafast performance**
  - **Capable of 100-Gb/s bitwise switching, 640-Gb/s wavelength conversion**
- **Channel-rate processing**
  - **No demultiplexing to lower bit-rates**
- **Fewer O/E/O conversions**
- **Network flexibility**
  - **Payload transparency to bit rate & modulation format**

➡ **Decrease size, power, weight** ➡ **COST**

Outline

- **Motivation/Background: Routing and Regeneration**
- Ultrafast all-optical logic gates
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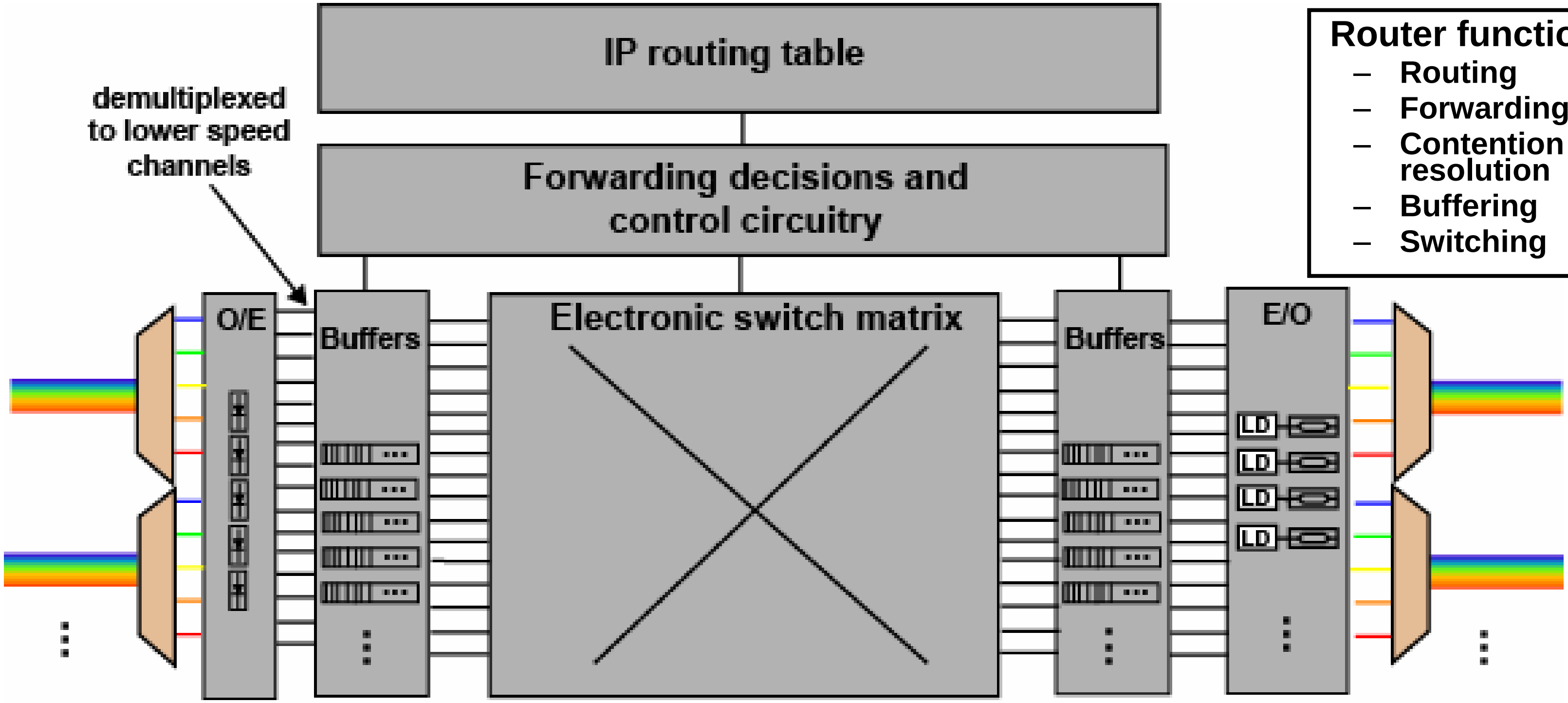
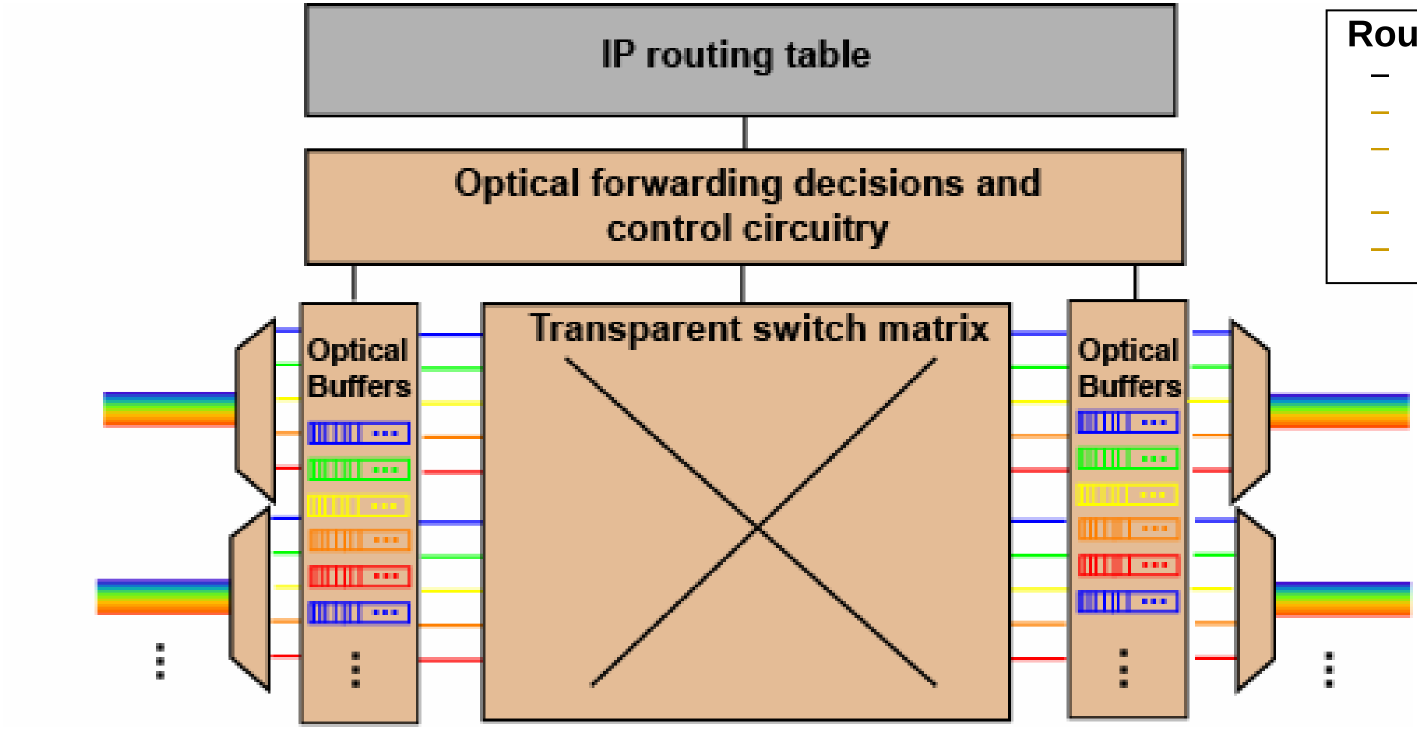
Routers: All Electronic



Router functions:
- Routing
- Forwarding
- Contention resolution
- Buffering
- Switching

- **Challenges with increasing bit rates:**
  - Limited electronic switch speeds (10-40 Gb/s)
  - Requires multiple lower-speed channels
  - Duplication of low-speed O/E/O, buffers, switches
  - Requires conversion and storage of every bit

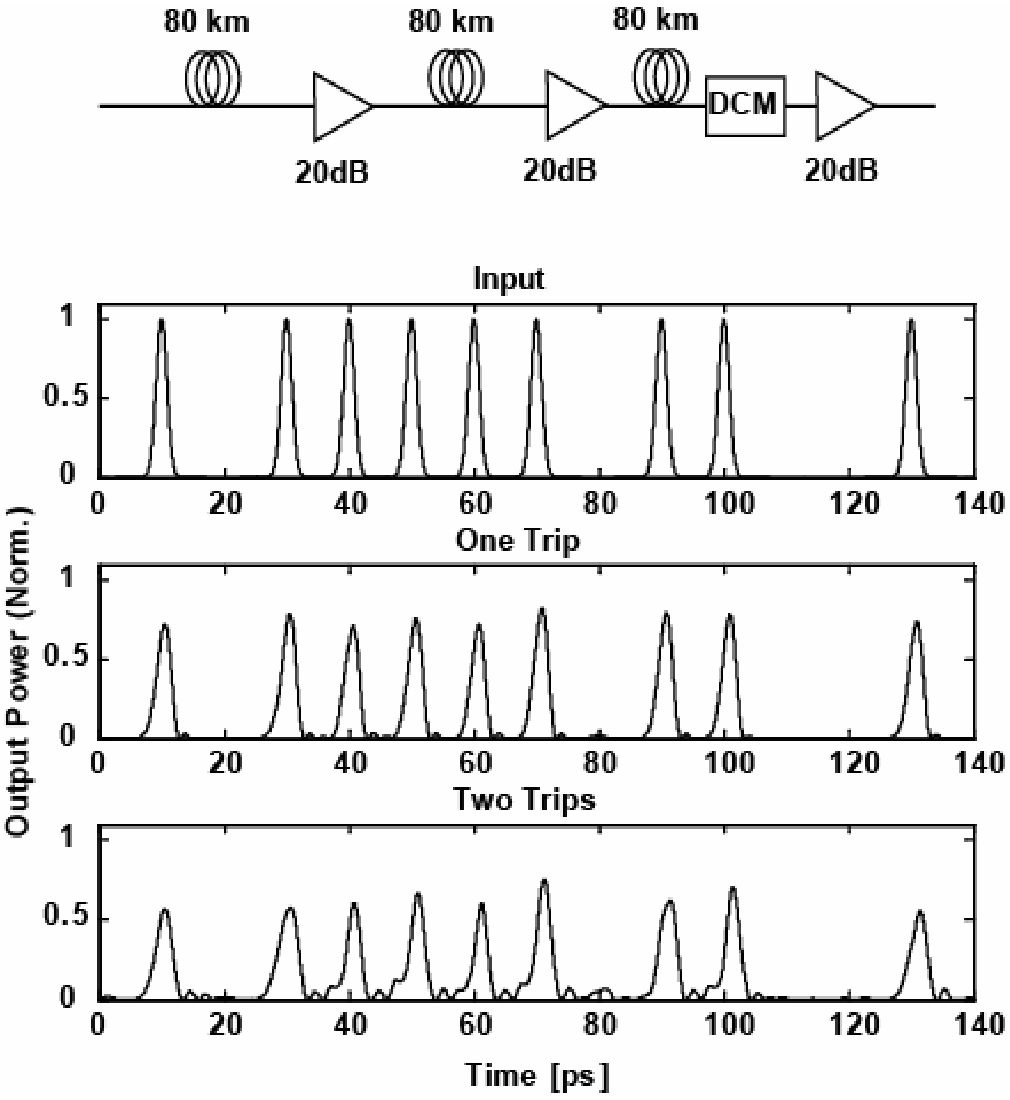
Routers: All-Optical Header Processing



Router functions:
- Routing
- Forwarding
- Contention resolution
- Buffering
- Switching

- **All-optical payload path:**
  - High-speed optical switching capable of channel-rate processing
  - Reduce O/E/O conversions (reduce size, weight, and power consumption)
  - Offers payload transparency for flexible networking
- **All-optical packet processing:**
  - Reduce packet processing latencies
  - Minimize buffering requirements

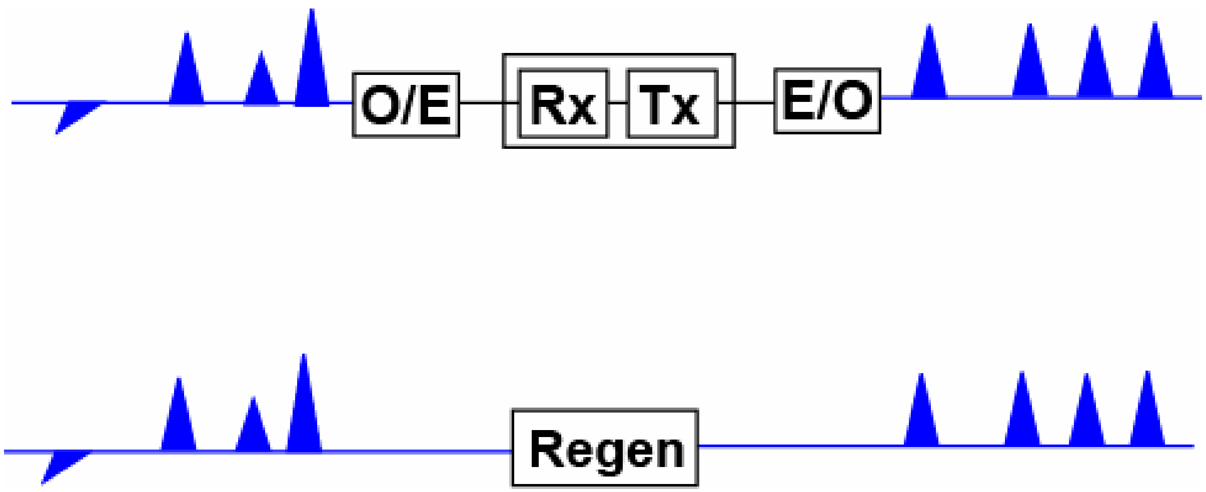
The Need for Regeneration



- Linear and nonlinear effects in optical fiber
- Dispersion compensation cancels 2nd order dispersion
- Amplifiers compensate for loss
- Amplitude variation
- Pulse shape distortion
- Timing jitter (not simulated)
  - Due to amplifier and transmitter noise

Electronic and Optical Regeneration

Re-Amplify
Re-Time
Re-Shape
Re-Polarize



- **All-optical regenerator**
  - **High-speed optical switching capable of channel-rate processing**
  - **Reduce O/E/O conversions**
  - **Size, weight, power improvements**

Challenges for All-Optical Signal Processing

- **Challenges**
  - Electronic technology more mature and offers more functionality than optical switches
  - Optical switches still costly compared with electronic techniques
- **This thesis**
  - Demonstrate increased functionality for all-optical processing
  - Improve practicality of all-optical logic gates

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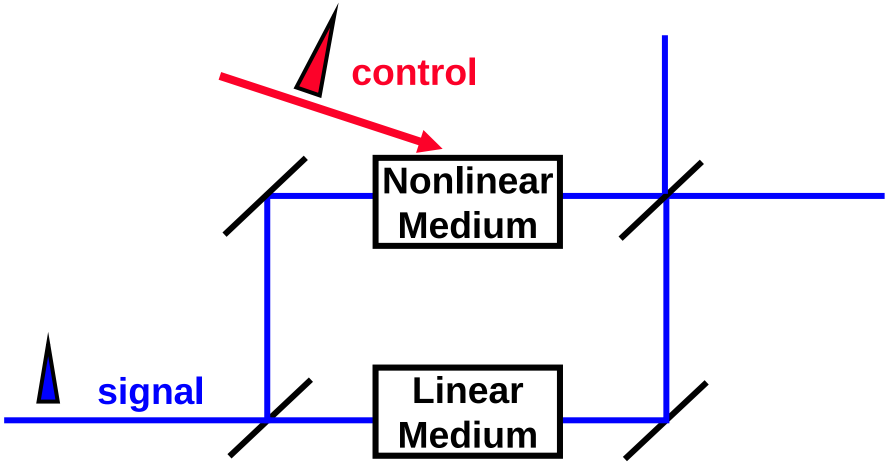
Ultrafast Interferometric All-Optical Switching

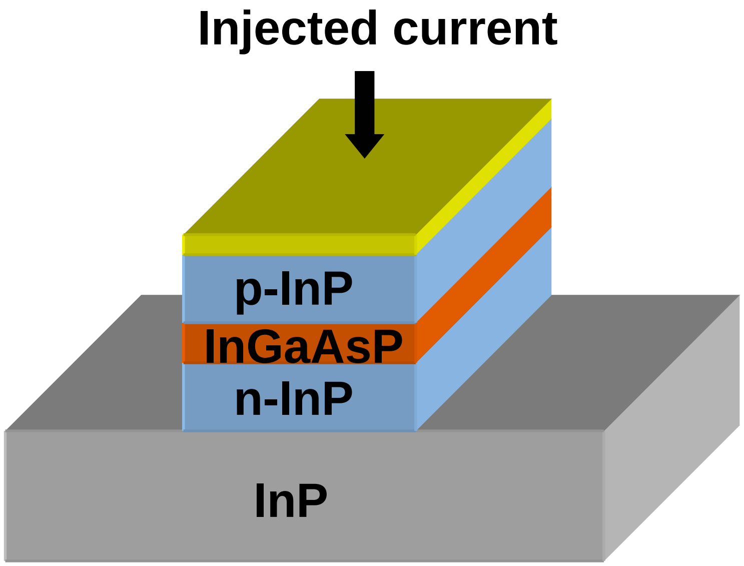


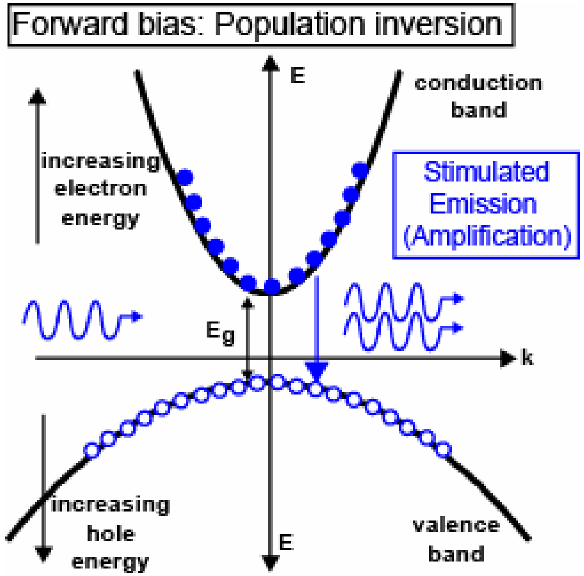
- Interferometric switch: change index of refraction (phase)
- Ultrafast performance
- Spatial switching

- Fiber
  - Weak nonlinearity (10^{-16} cm^2/W)
  - Fast response (~fs)
  - No integration – long lengths required
- Photonic crystal fiber, highly nonlinear fiber
  - Fast, strong nonlinearity
  - Integration potential?

- Semiconductor optical amplifier
  - Strong nonlinearity (~10^{-12} cm^2/W)
  - Slow recovery time (~ 100 ps)
  - Potential for integration (semiconductor processes)
- Quantum dot SOA
  - Fast recovery time (~10 ps)
  - Strong nonlinearity?

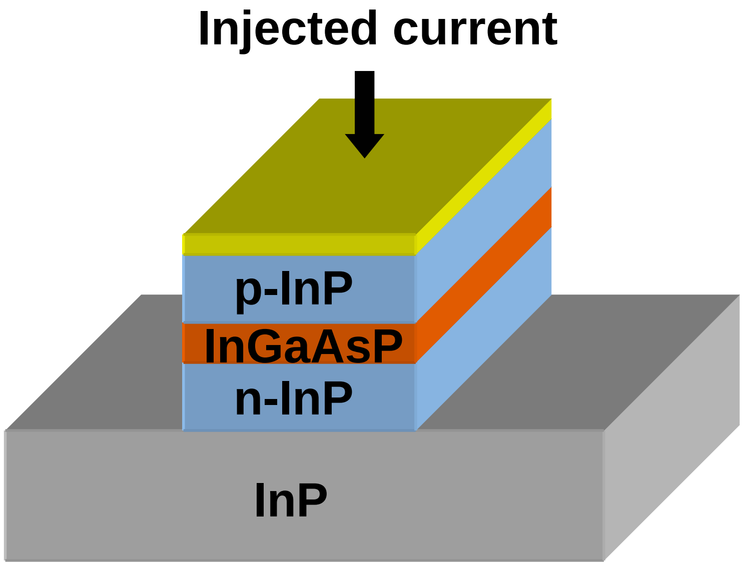
SOA Operation

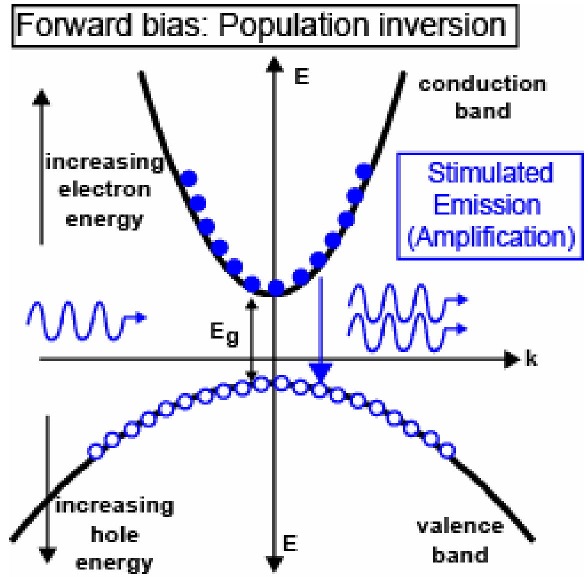




- Interaction of optical waves with SOA carriers
  - Stimulated recombination of electrons and holes creates gain
  - Optical waves change carrier distribution
  - Changes gain and index of refraction → optical switching

SOA Operation



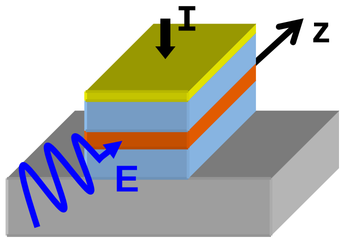


- **Interaction of optical waves with SOA carriers**
  - **Stimulated recombination of electrons and holes creates gain**
  - **Optical waves change carrier distribution**
  - **Changes gain and index of refraction → optical switching**
- **How does the incident light affect the carrier density?**
  - **Phenomenological model**
  - **Focus on time scales ~ 10 ps (100 Gb/s)**

A Phenomenological Model

Key assumptions: $\text{gain} = a(N - N_o)$

$\text{index} = \alpha \cdot \text{gain}$



V = volume
N = carrier density

Rate equation describing carrier evolution

$$\frac{\partial N}{\partial t} = D\nabla^2 N + \frac{I}{qV} - \frac{N}{\tau_c} - \frac{a(N - N_o)}{\hbar\omega}|E|^2,$$

Carrier diffusion

Current injection

Spontaneous recombination

Stimulated recombination

G. P. Agrawal and N. A. Olsson, IEEE J. Quantum Electronics, 25 (11), 1989.

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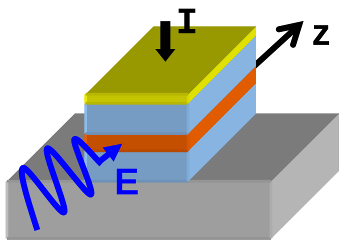

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Wave equation describing optical propagation

$$\nabla^2 E - \frac{\varepsilon}{c^2}\frac{\partial^2 E}{\partial t^2} = 0,$$

Background index

$$\varepsilon = n_o + \chi(N)$$

Index of refraction

$$\chi(N) = -\frac{\overline{n}c}{\omega_o}(\alpha + i) \cdot a(N - N_o)$$

Gain/Loss

G. P. Agrawal and N. A. Olsson, IEEE J. Quantum Electronics, 25 (11), 1989.

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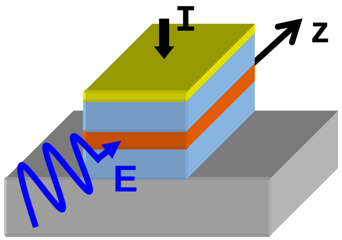

V = volume
N = carrier density
h(τ) = integrated gain

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Coupled equations describing gain evolution, optical pulse amplitude and phase propagation

$$h(\tau) = \int_0^L g(z,\tau)dz$$

$$\frac{\partial h(\tau)}{\partial \tau} = \frac{g_o L - h(\tau)}{\tau_c} - \frac{P_{in}(\tau)}{E_{sat}}\left(e^{h(\tau)} - 1\right)$$

$$P_{out}(\tau) = P_{in}(\tau)e^{h(\tau)}$$

$$\Phi_{out}(\tau) = \Phi_{in}(\tau) - \frac{1}{2}\alpha h(\tau)$$

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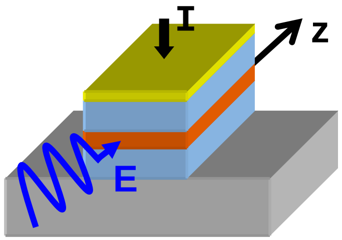

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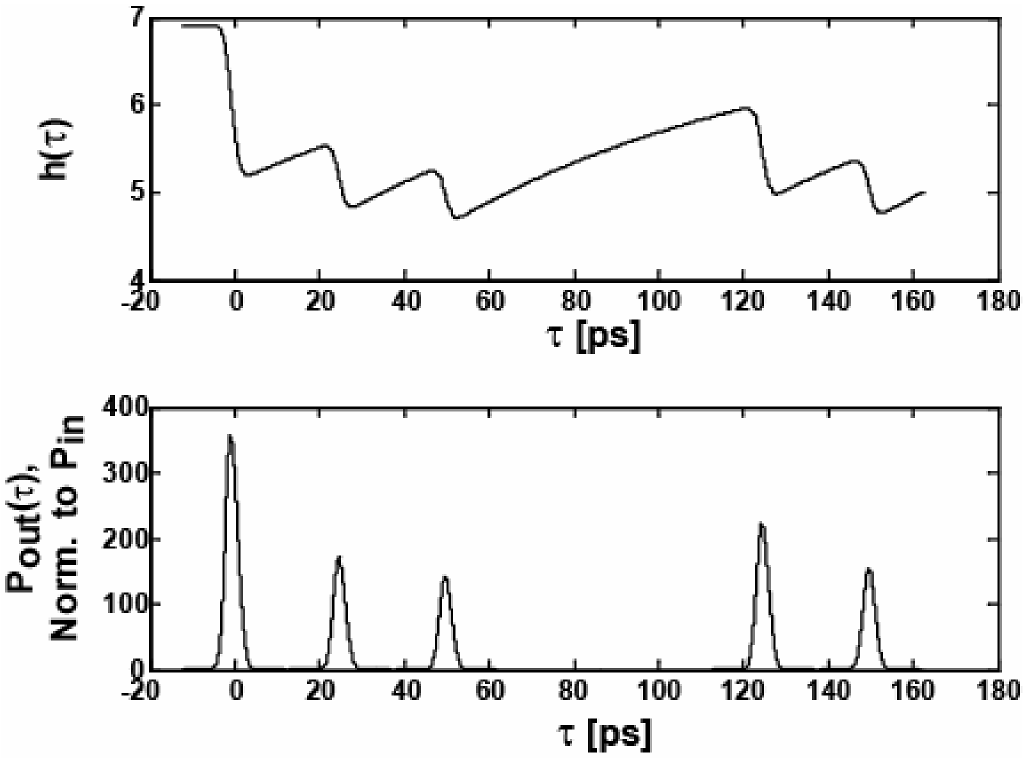
- **Gain saturates and recovers**
- **Phase $\propto$ gain**

G. P. Agrawal and N. A. Olsson, IEEE J. Quantum Electronics, 25 (11), 1989.

Carrier Recovery Time Limitation

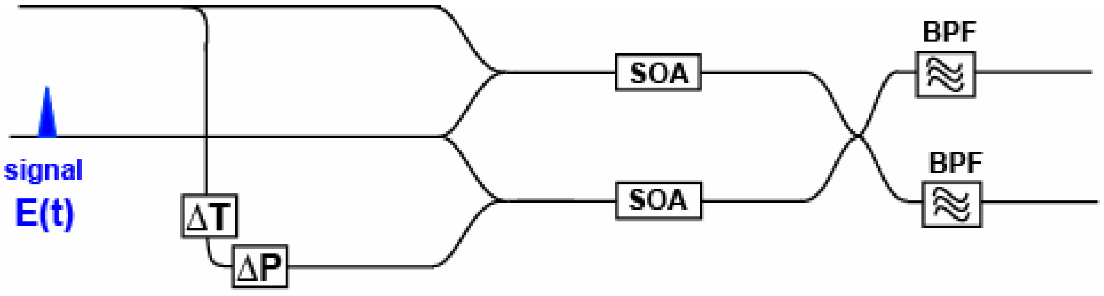


- 2-ps pulses, 40 Gb/s
- 5 fJ input pulse energy

- τ_c = 80 ps
- Initial gain: 30 dB
- L = 1 mm
- E_{sat} = 1 pJ
- α = 5

- Long carrier recovery time creates pulse patterning
- Limits switching speed to ~10 Gb/s
- Solution: balanced interferometer approach

Balanced Interferometer Design



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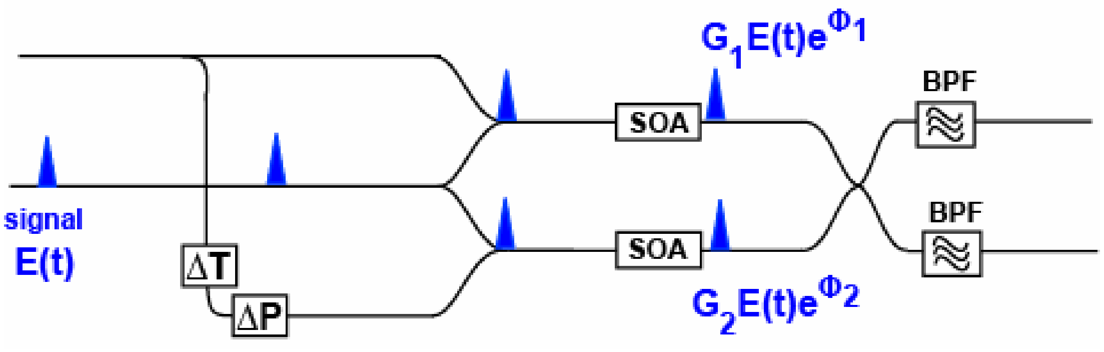

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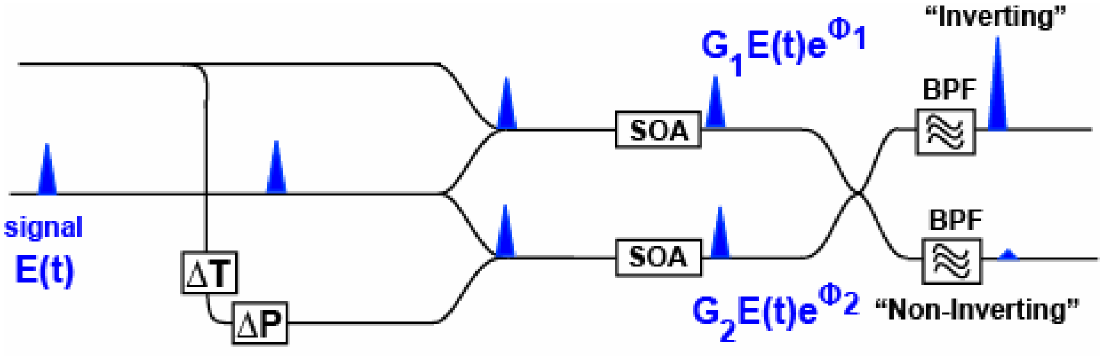

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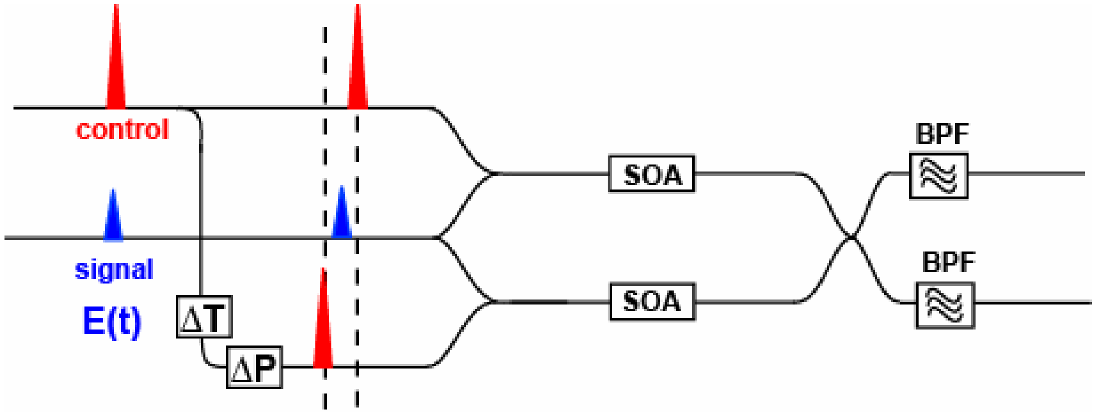

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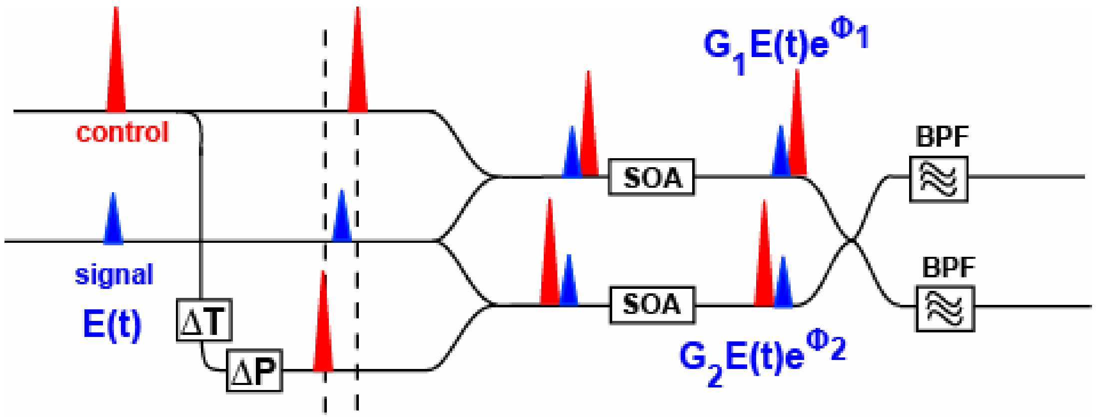

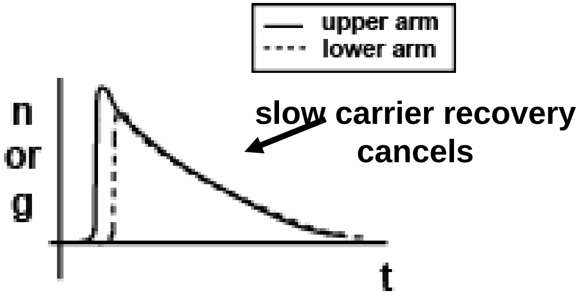

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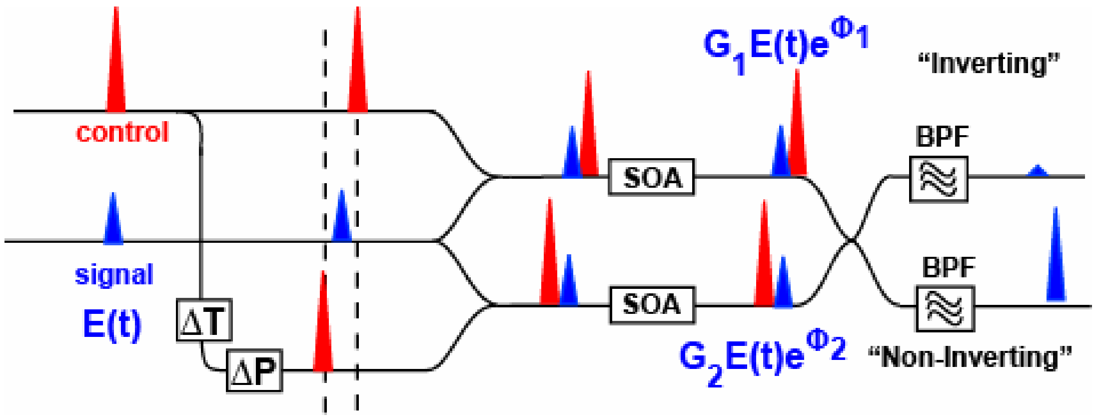

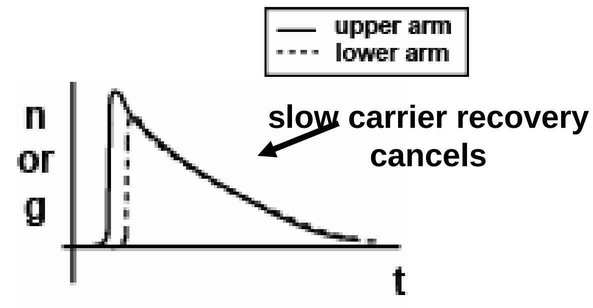

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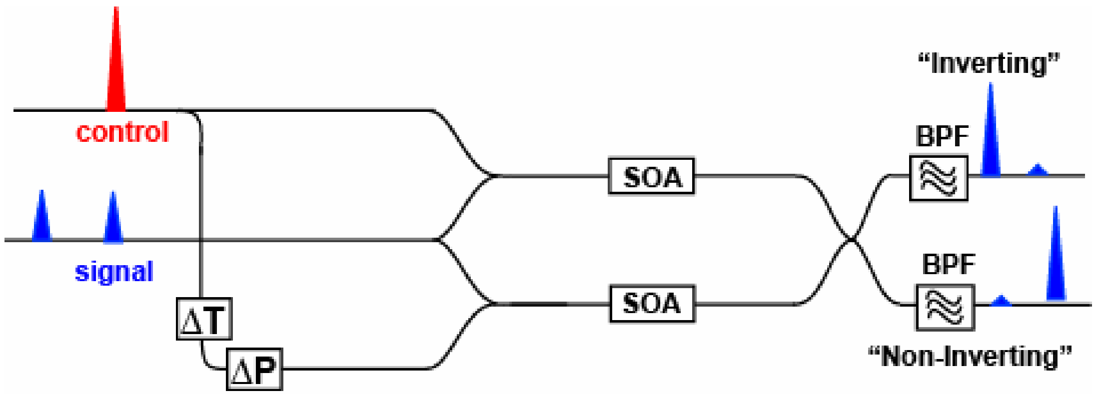
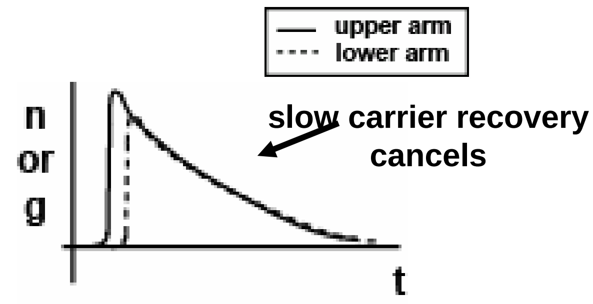
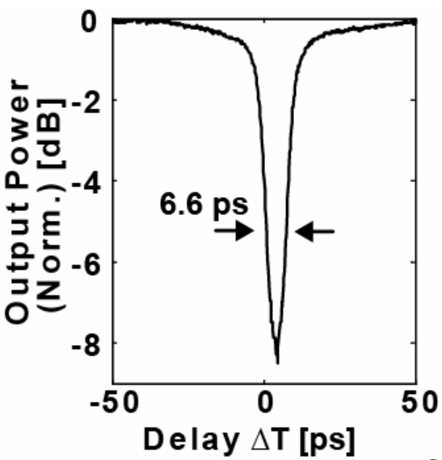
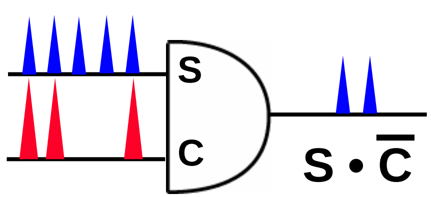




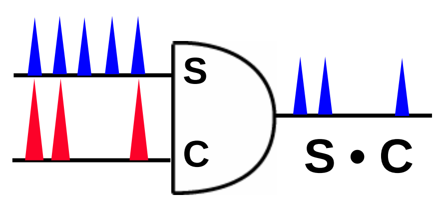
Inverting





2-ps signal and control pulses

Non-inverting



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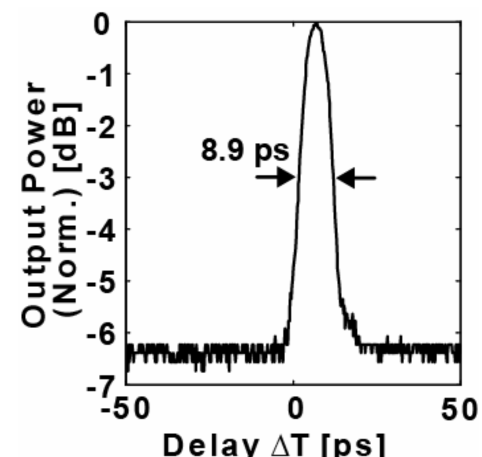

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- **Routing: 40-Gb/s all-optical header processing**
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40-Gb/s All-Optical Header Processing

- **Goal: Demonstrate ultrafast packet processing functionality for routing**

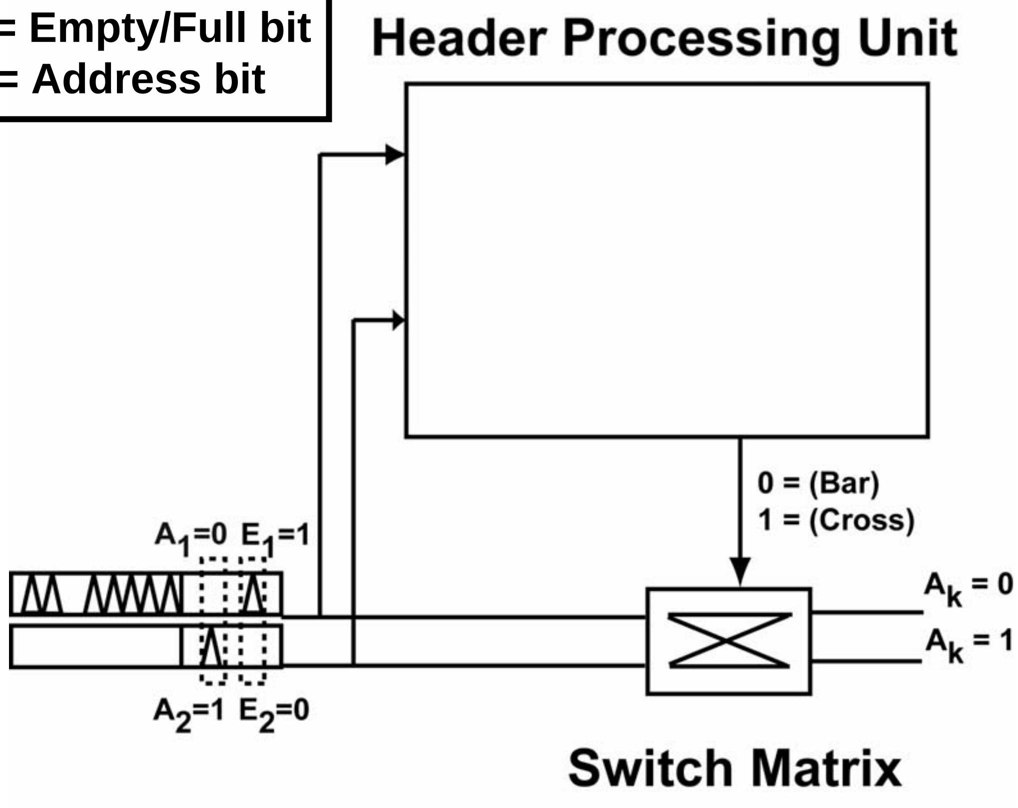
- **Previous work*:**
  - **Ultrafast all-optical header processing of single packets**
  - **Applicable to add/drop nodes, ring networks**

- **This work:**
  - **Multi-packet all-optical header processing demonstration**
  - **Scalable topology: can be easily extended to larger switches**
  - **Applicable to wide variety of networks, including multi-degree mesh nodes**
  - **Increased packet processing functionality**

*Cardakli et al. (2000), Glesk et al. (1994), Cotter et al. (1995), Hamilton et al. (2002), Ramos et al. (2005).

Header Processing Logic

E_k = Empty/Full bit
A_k = Address bit



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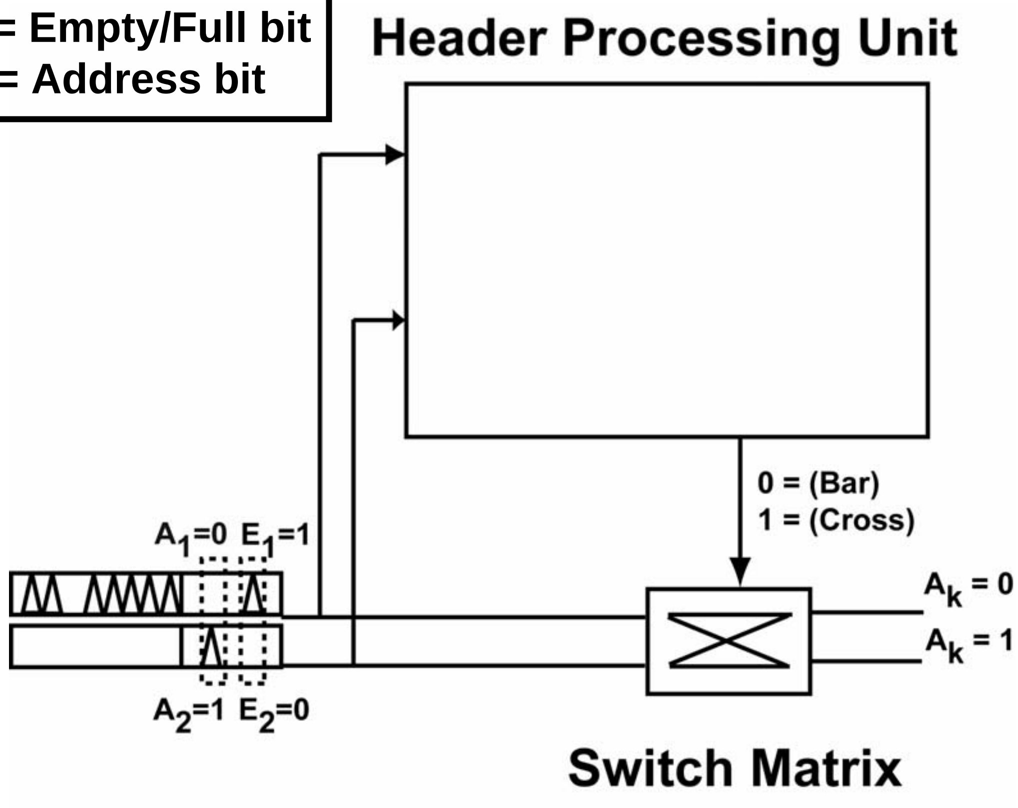

E_1E_2 \ A_1A_2	00	10	11	01
00	X	X	X	X
10	0	1	1	0
11	X	1	X	0
01	1	1	0	0

Header Processing Logic

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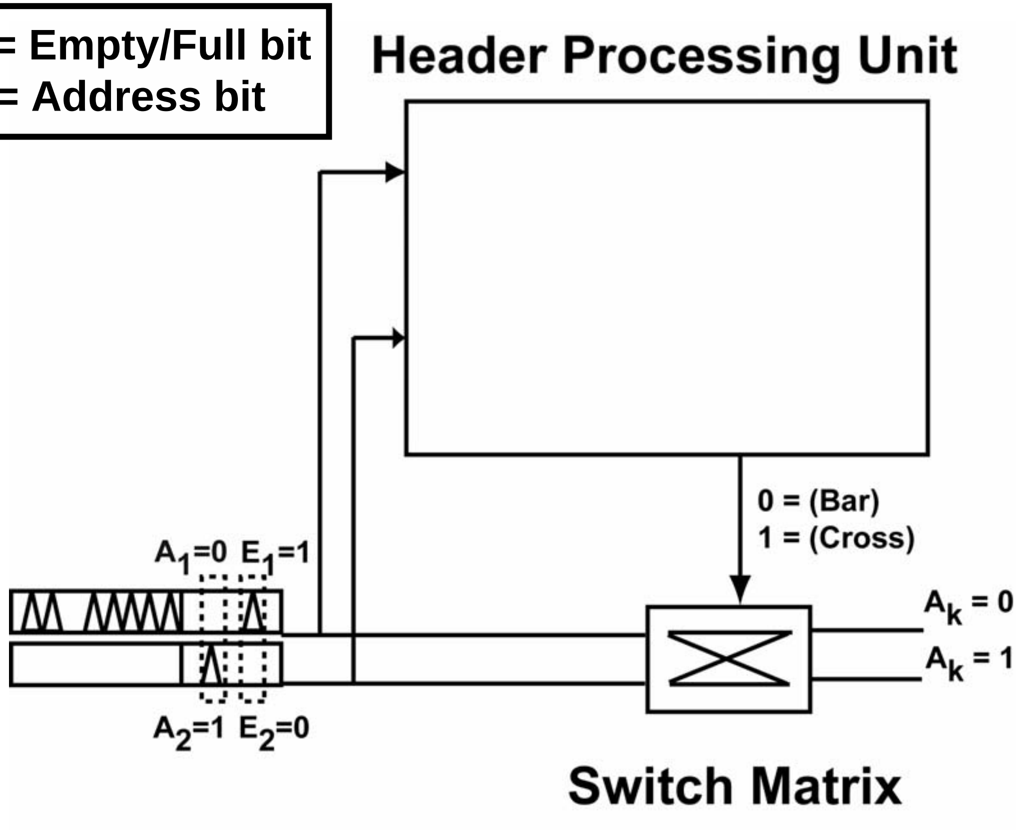

E_1E_2 \ A_1A_2	00	10	11	01
00	X	X	X	X
10	0	1	1	0
11	X	1	X	0
01	1	1	0	0

$$R = A_1 \cdot E_1 + \overline{A}_2 \cdot E_2$$

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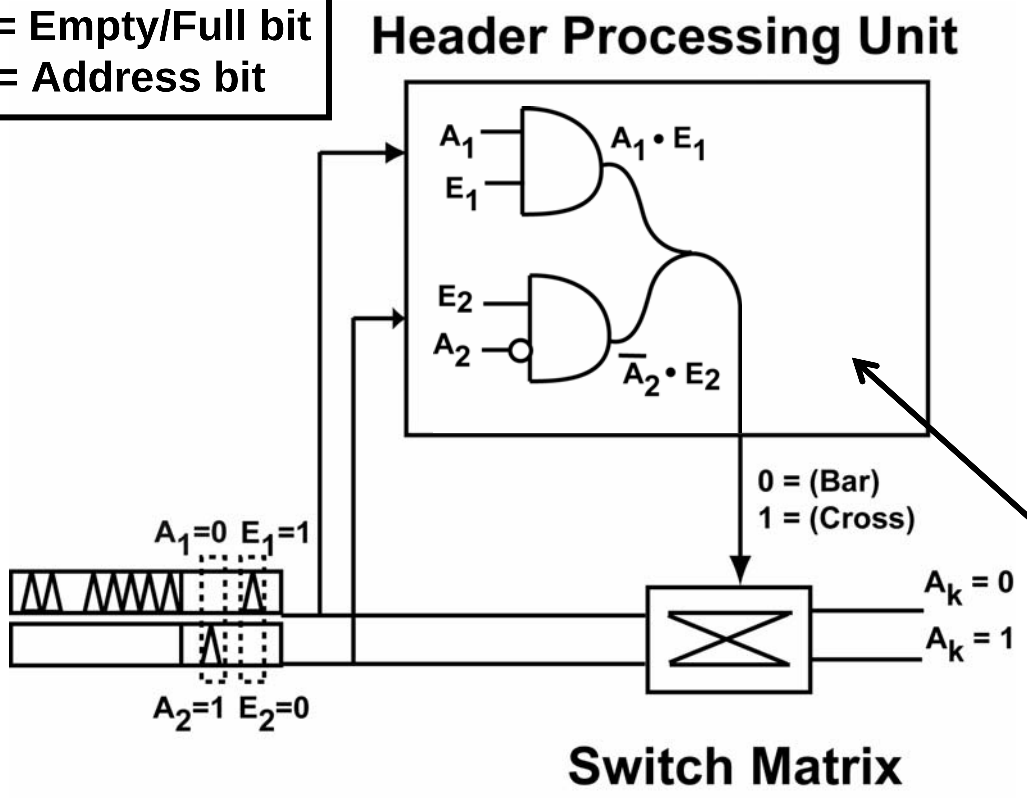

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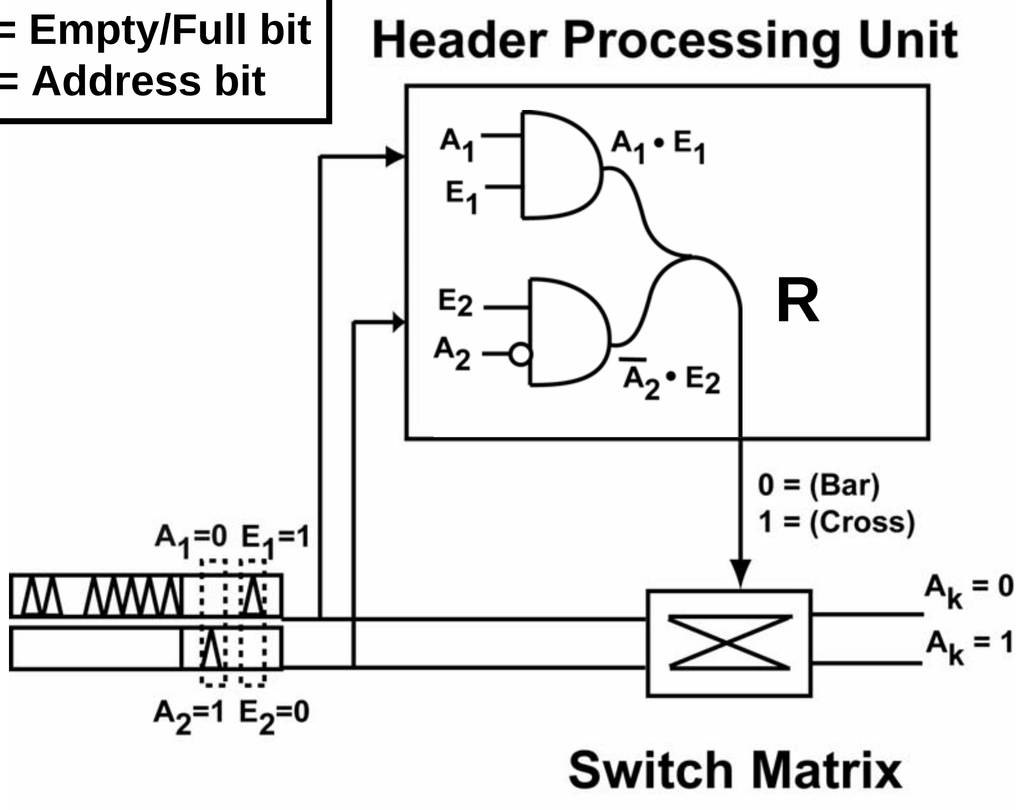
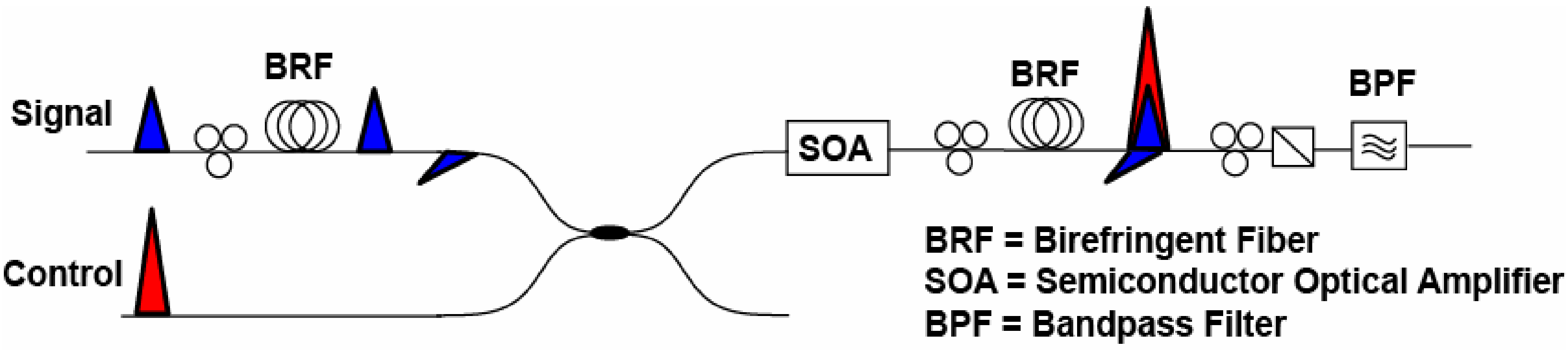


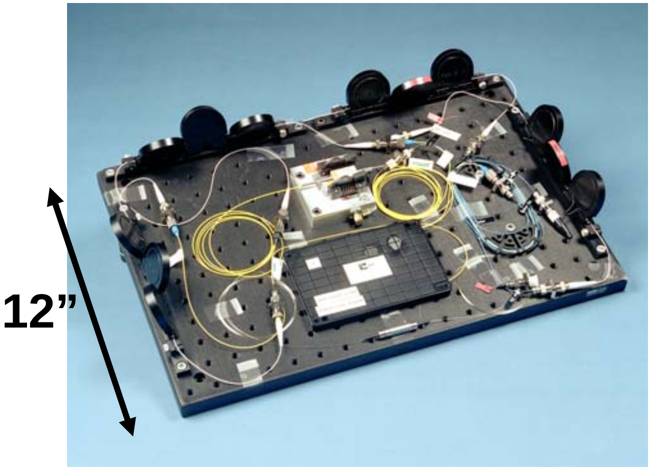
E_1E_2 \ A_1A_2	00	10	11	01
00	X	X	X	X
10	0	1	1	0
11	X	1	X	0
01	1	1	0	0

$$R = A_1 \cdot E_1 + \overline{A_2} \cdot E_2$$

- Multi-packet processing (2 incoming packets to 2 outgoing ports)
- Scalable: 2 optical logic gates for each 2x2 switch
- Potential for integration (SOA-based logic)

Optical Logic Gate Implementation: Ultrafast Nonlinear Interferometer (UNI)





N. S. Patel, K. L. Hall, and K. A. Rauschenbach, Optics Letters, 21 (18), 1996.

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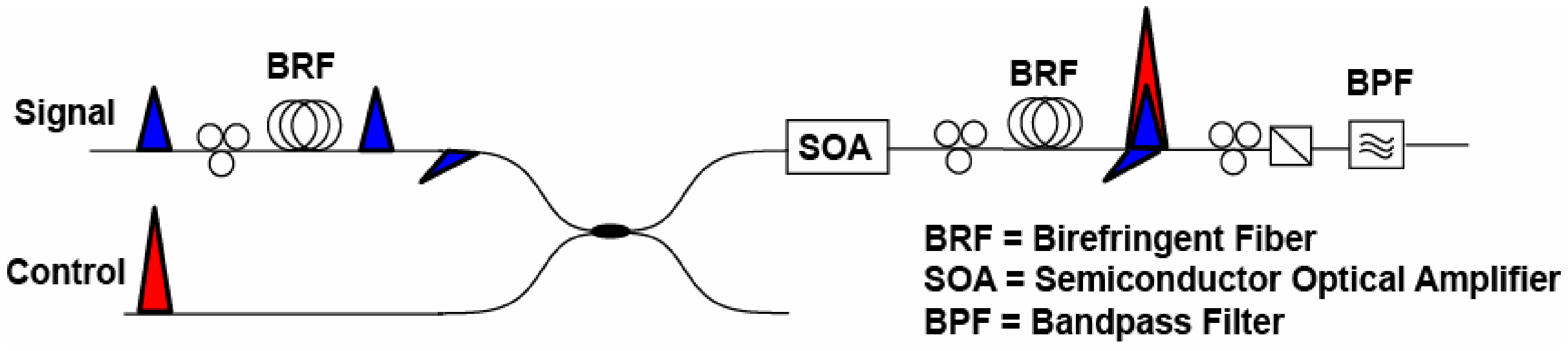
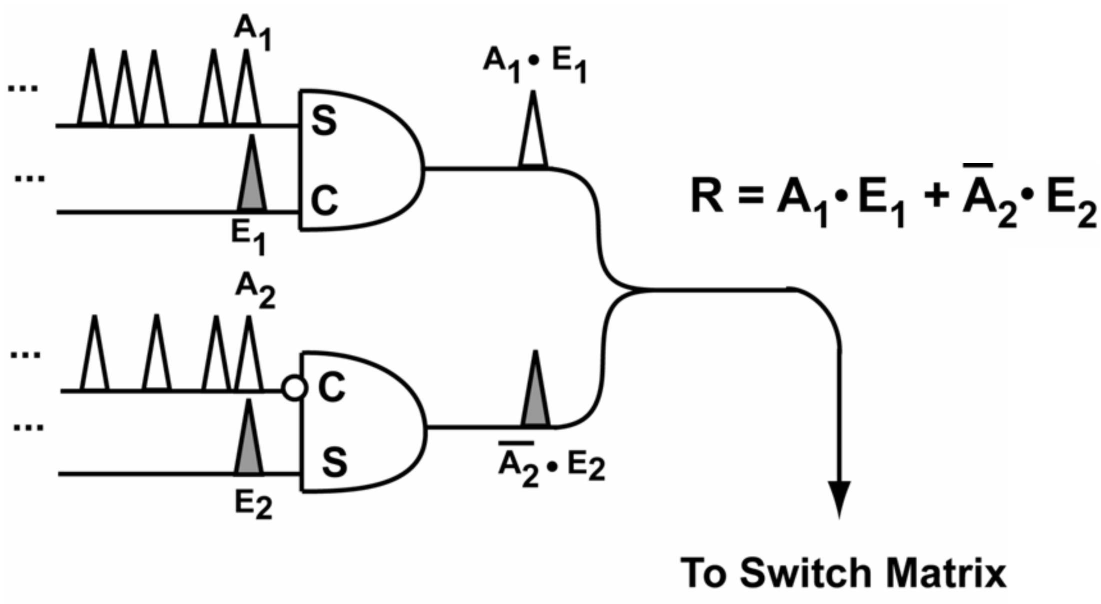
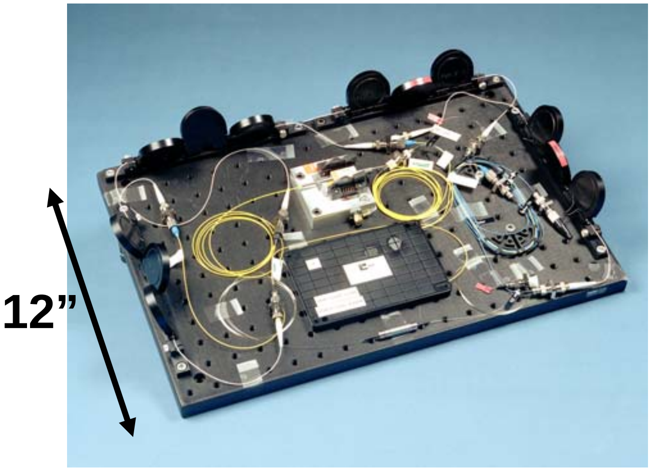
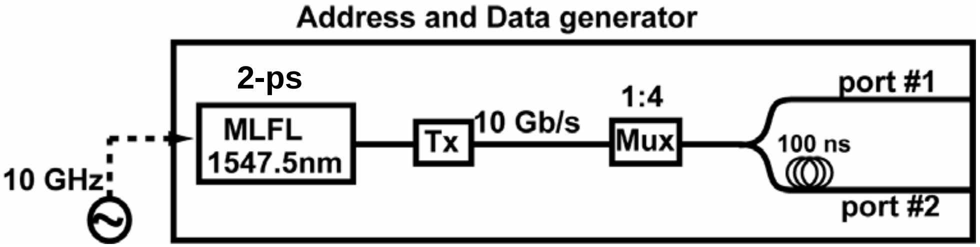




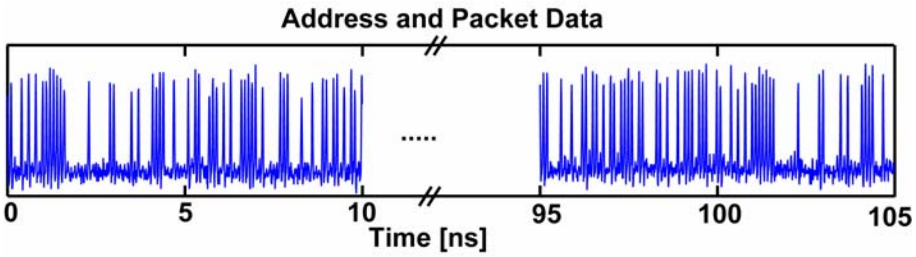


N. S. Patel, K. L. Hall, and K. A. Rauschenbach, Optics Letters, 21 (18), 1996.

Full System Experimental Schematic

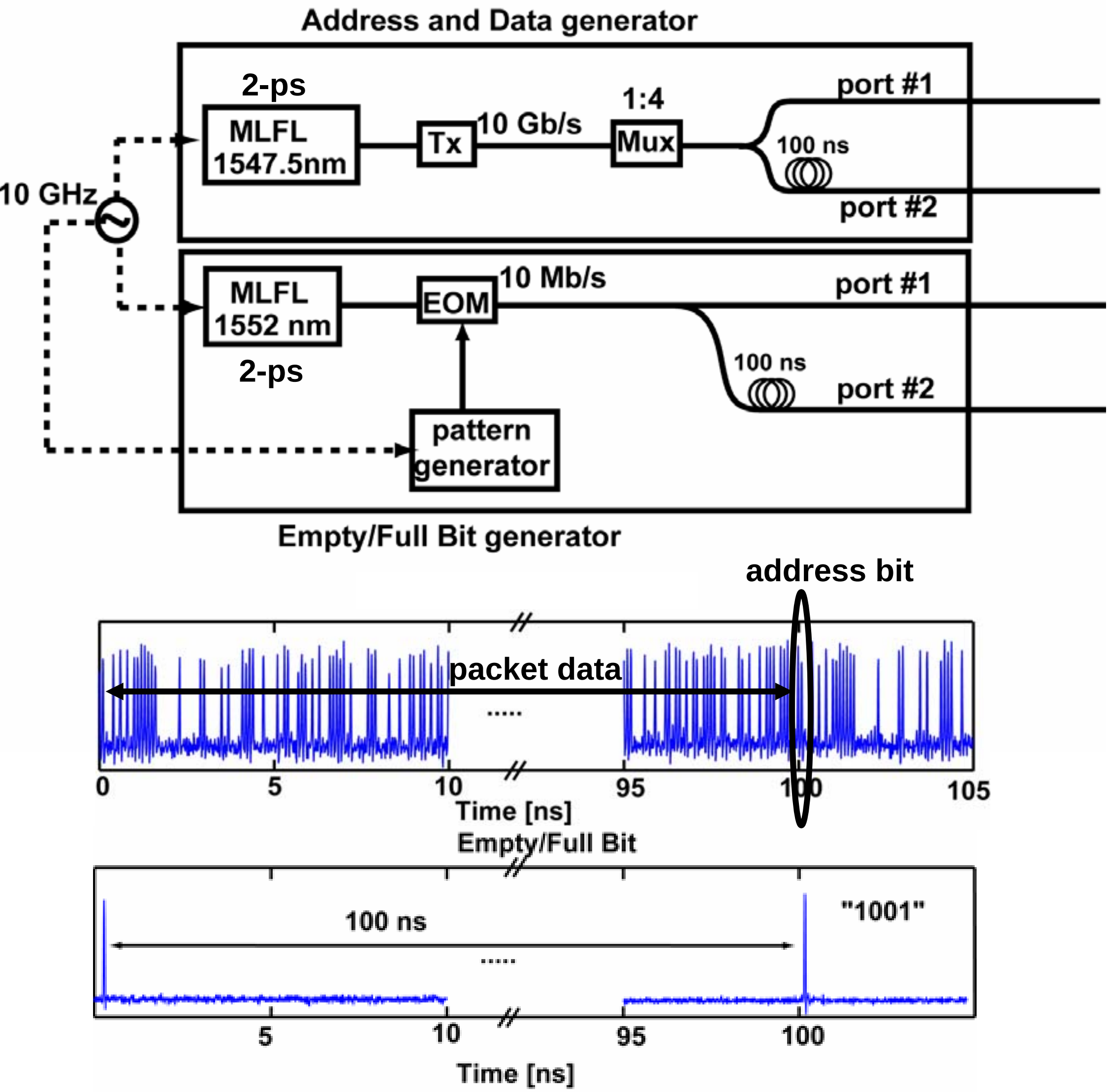


MLFL = Mode-locked Fiber Laser
Tx = Transmitter



- Packet Architecture
  - 2^7-1 PRBS

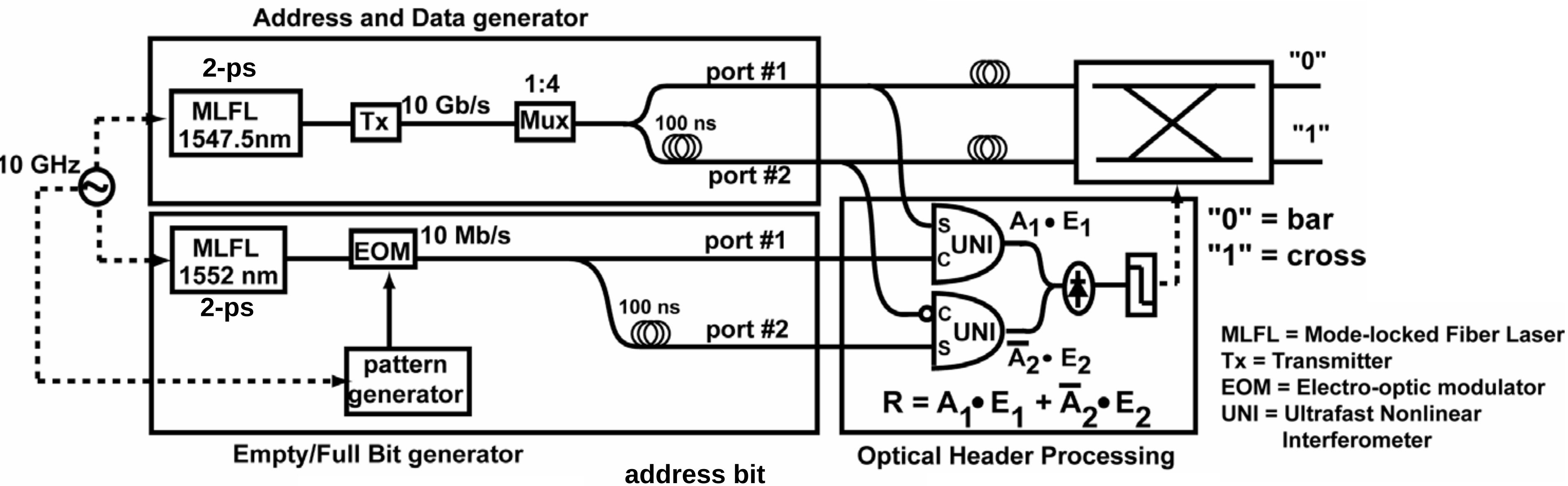
Full System Experimental Schematic

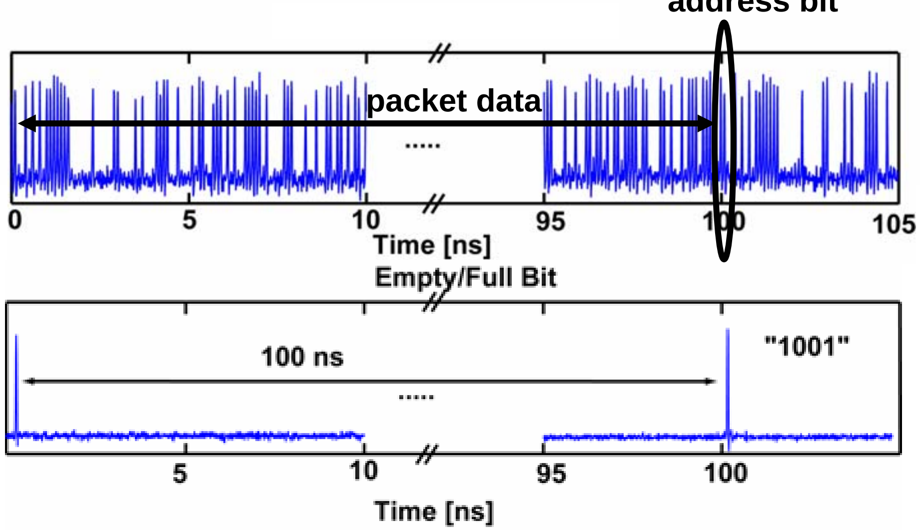


MLFL = Mode-locked Fiber Laser
Tx = Transmitter
EOM = Electro-optic modulator

- Packet Architecture
  - 2^7-1 PRBS
  - 4000 bits/packet
  - 100 ns packet

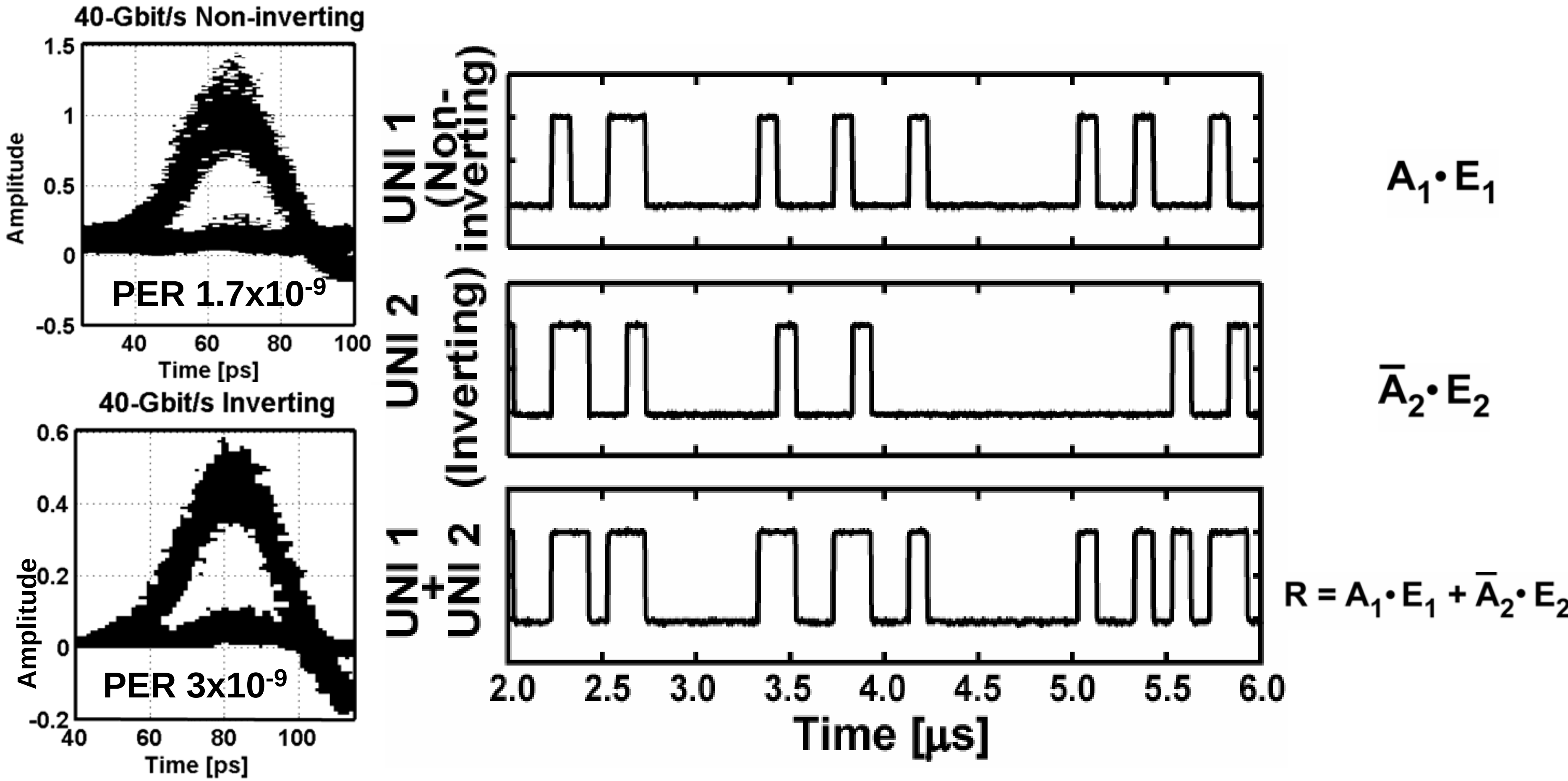
Full System Experimental Schematic





- Packet Architecture
  - 2^7-1 PRBS
  - 4000 bits/packet
  - 100 ns packet

Ultrafast All-Optical Header Processor

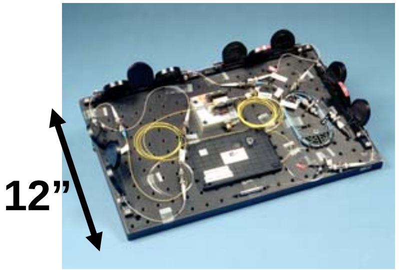


- **Ultrafast operation: Header error rate of 1×10^{-6} with 40-Gbit/s line rate**
- **Comparable with current electronic router error rates**
- **Low switching-energy: 60.5 fJ/packet**

J. Wang et al., “Demonstration of 40-Gb/s Packet Routing Using All-Optical Header Processing”, IEEE Photonics Technology Letters, 18 (21), 2006.

The Need For Integration

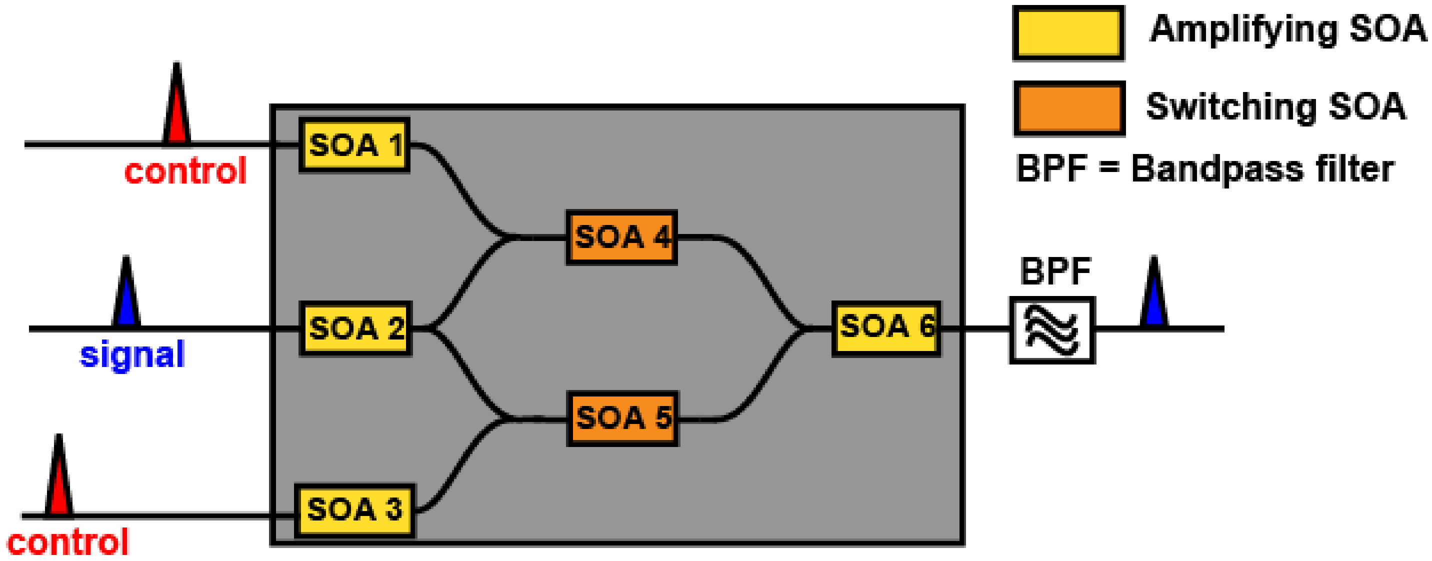
- **Successful demonstration of 2-port forwarding using discrete all-optical logic gates.**
- **What is required to expand this functionality?**
  - **Integration: Discrete logic gates are infeasible for practical implementation**
    - **Size, weight, cost**
    - **Ease of installation & operation**
  - **Simple method for optimizing each logic gate for optimal performance**
    - **Currently requires time-intensive search over a large parameter space**



Outline

- Motivation/Background
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
- **Performance optimization of optical logic gates**
- Regeneration
- Future SOA-MZI gates
- Conclusion

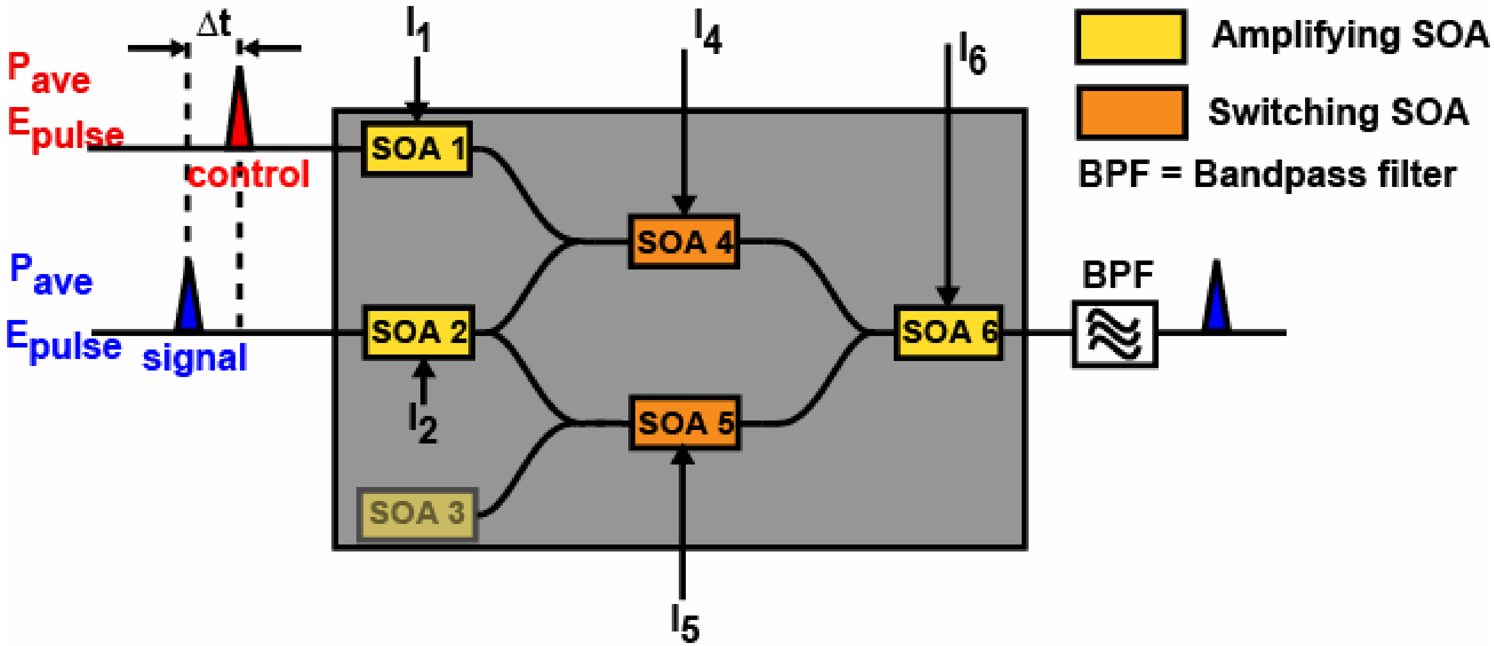
SOA Mach-Zehnder Interferometer: An Integrated Optical Logic Gate



- Integrated optical logic gate: SOA-MZI
- Conceptually similar to the UNI: balanced interferometer
- Waveguide and coupling losses require amplifying SOAs
- Complex parameter space makes optimization difficult

Developed by Alphion Corporation.

SOA Mach-Zehnder Interferometer: An Integrated Optical Logic Gate



- Focus on single-ended operation to observe SOA dynamics
- Key operating parameters
  - I_4, I_5
  - Signal and control average power

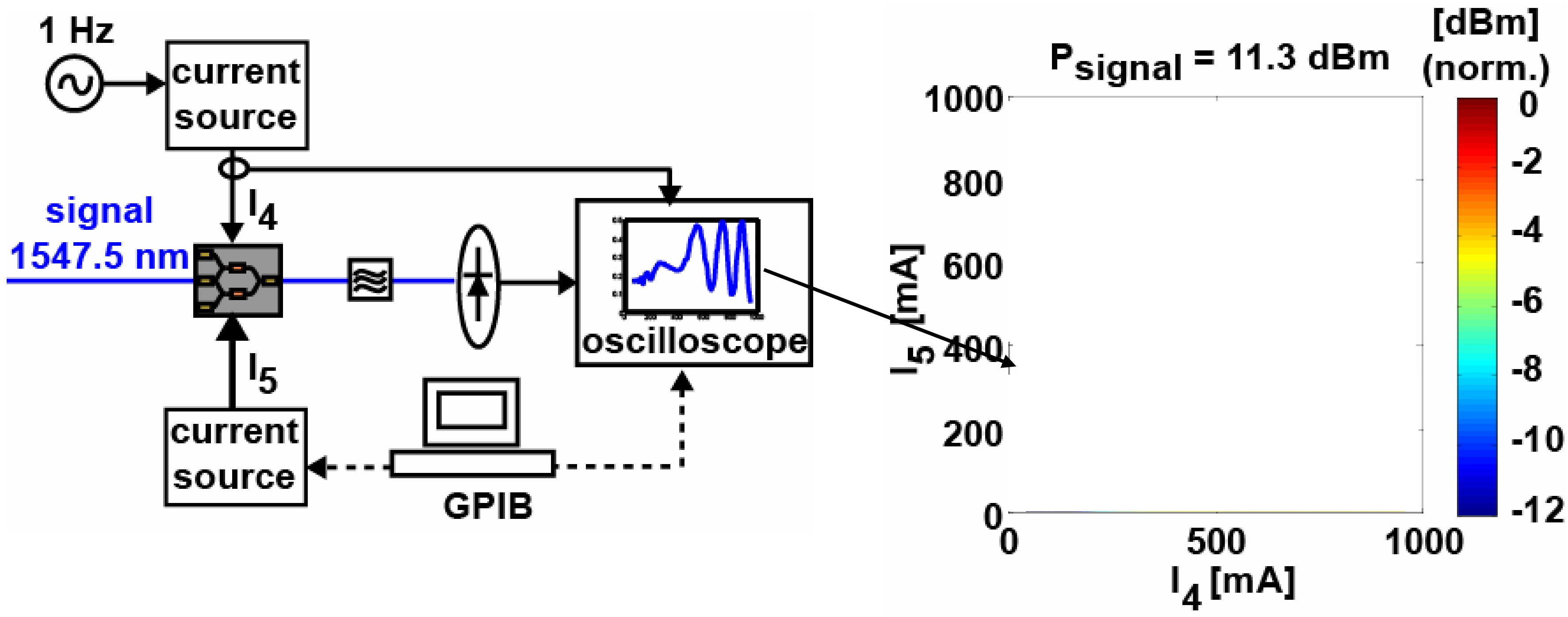
  } Static interferometer bias

  - Signal and control pulse power
  - Signal-control delay (Δt)

  } Switching dynamics

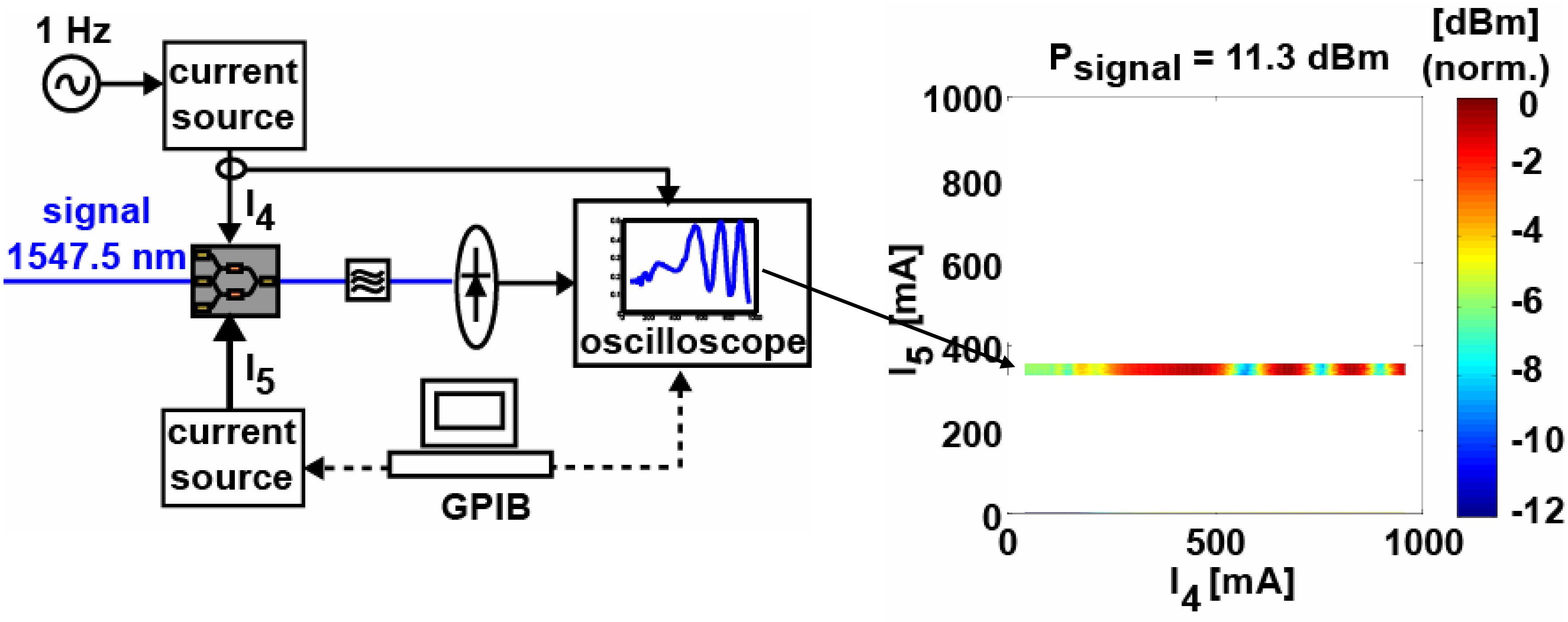
Developed by Alphion Corporation.

Static Interferometer Bias Map



- **Bias map measurement:**
  - Sweep I_4 current at 1 Hz
    - Measure current on SOA using hall-effect probe
  - Measure output power on oscilloscope
  - Full 2D scan taken on the order of minutes

Static Interferometer Bias Map



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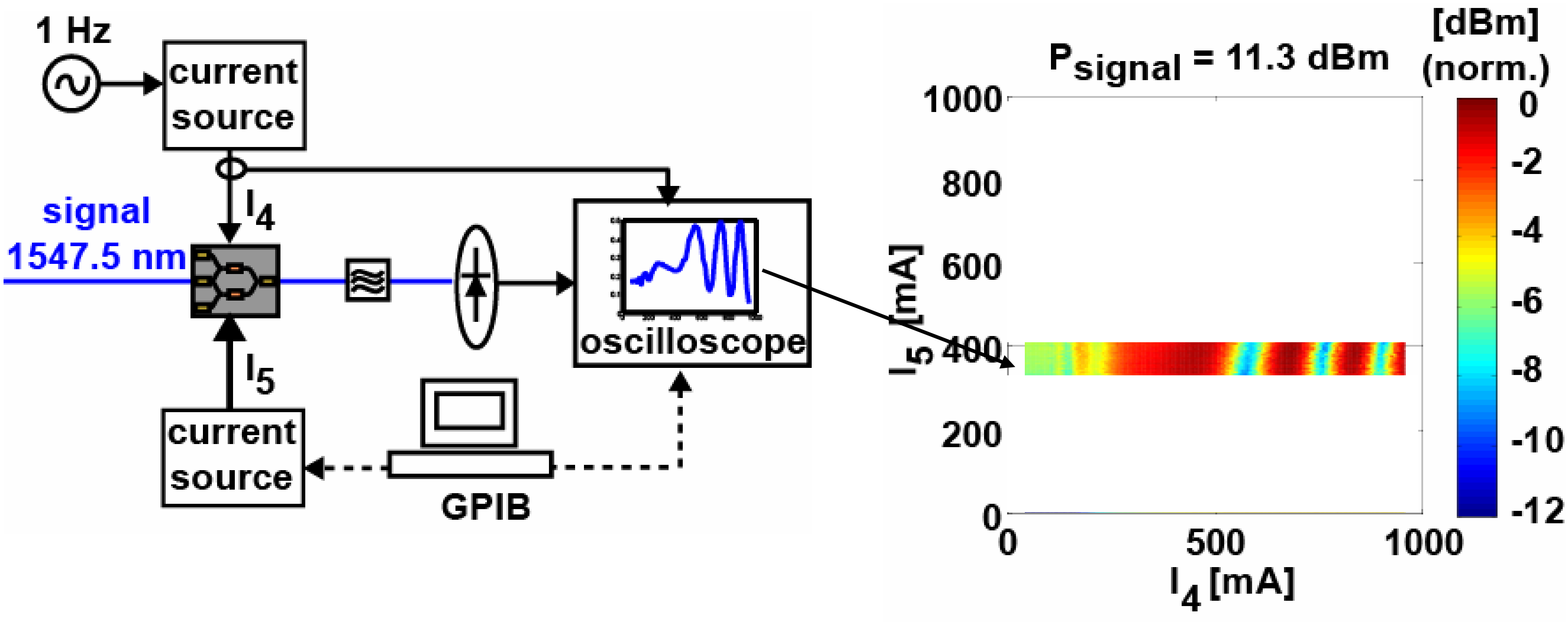

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MIT Lincoln Laboratory

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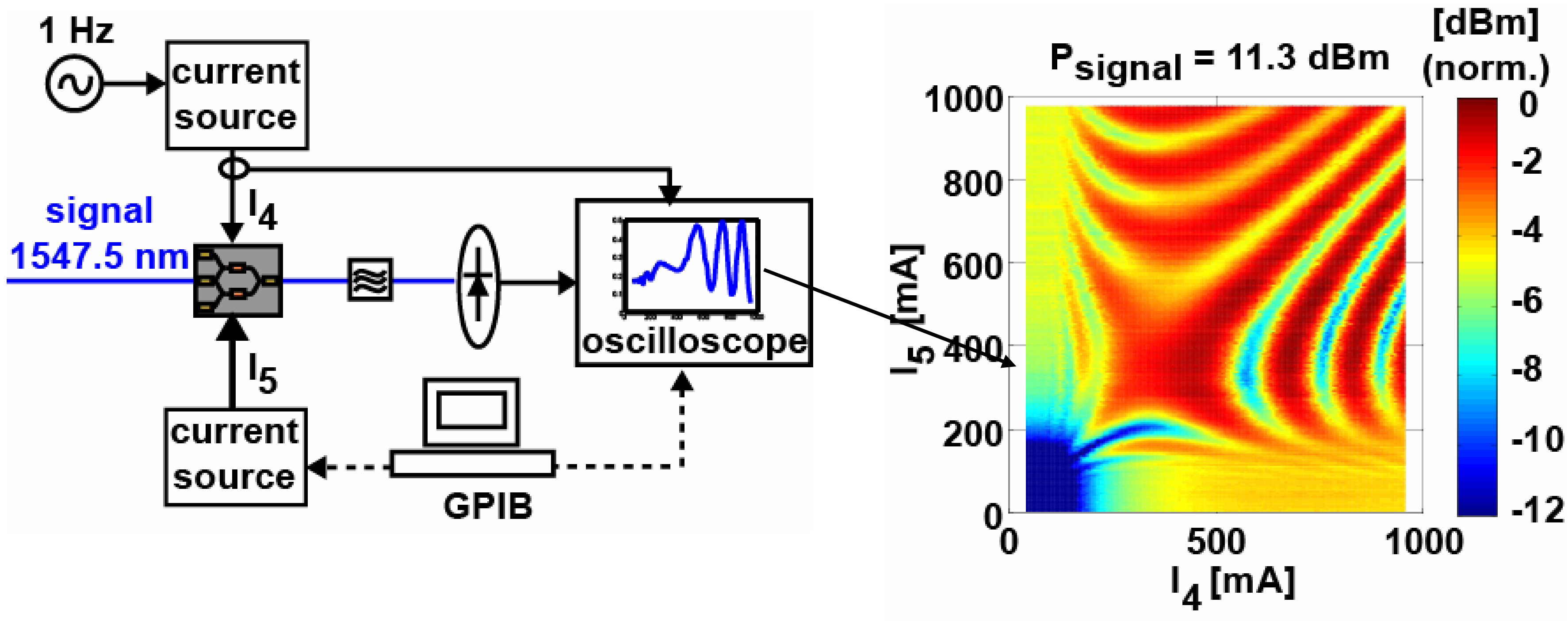

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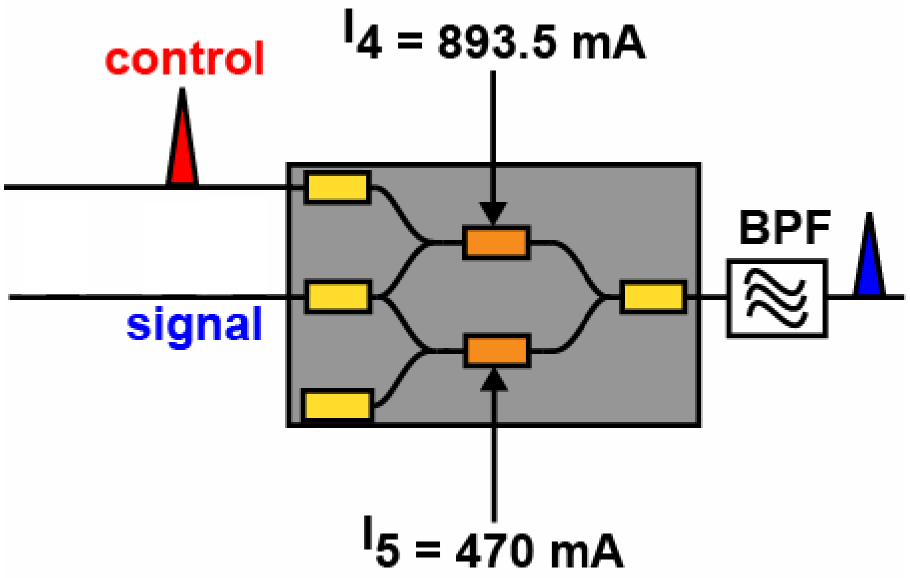
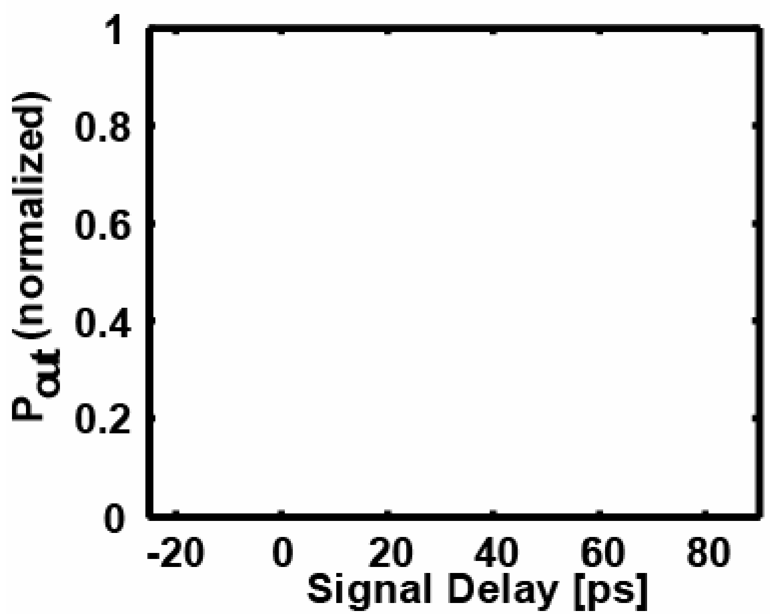
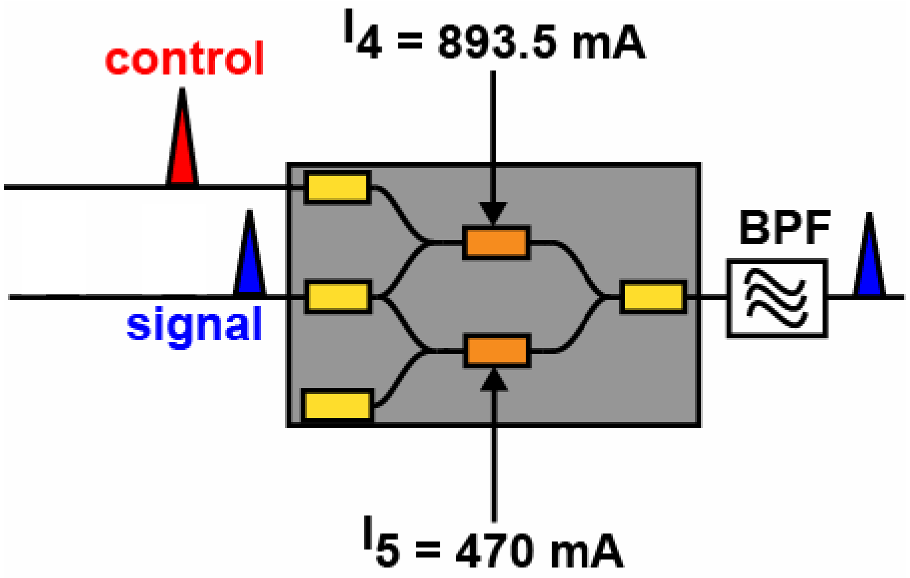
Switching Window Measurement

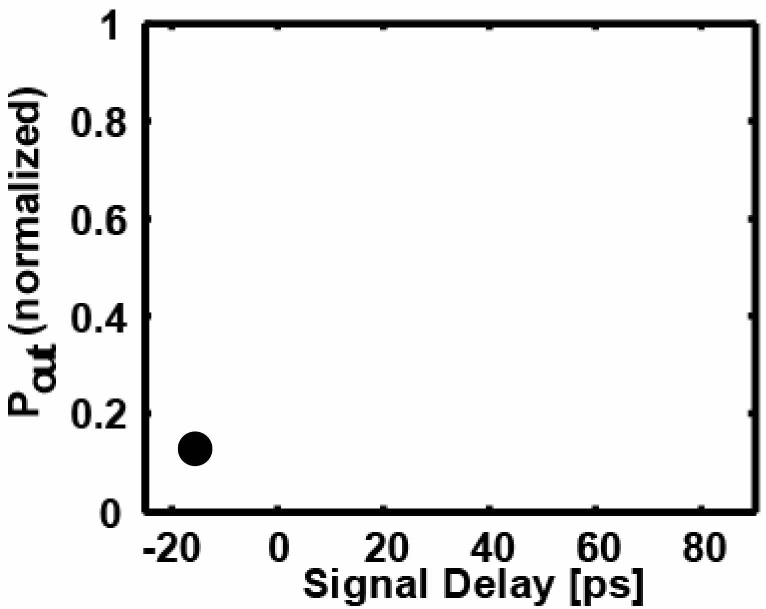




- Fix current bias (I_4, I_5)
- Measure average output power at every control-signal delay

Switching Window Measurement





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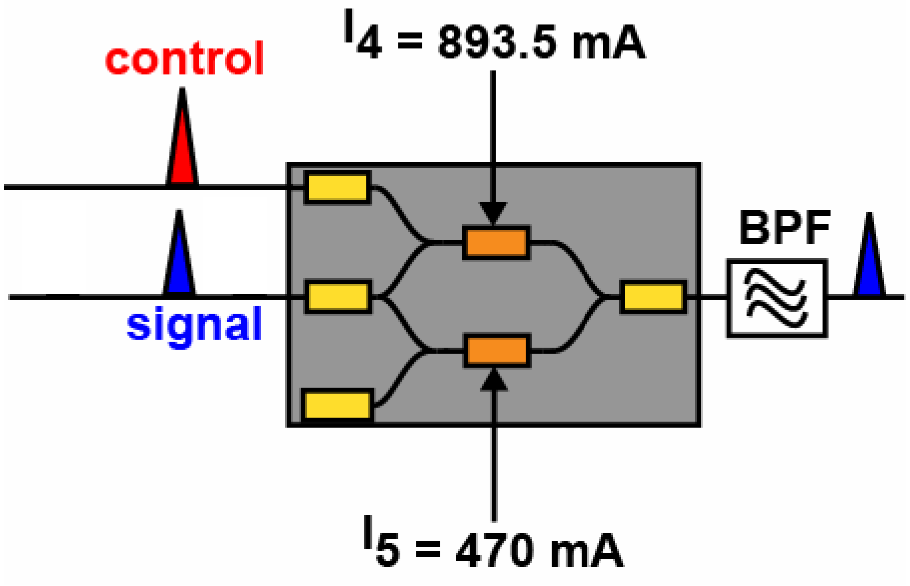

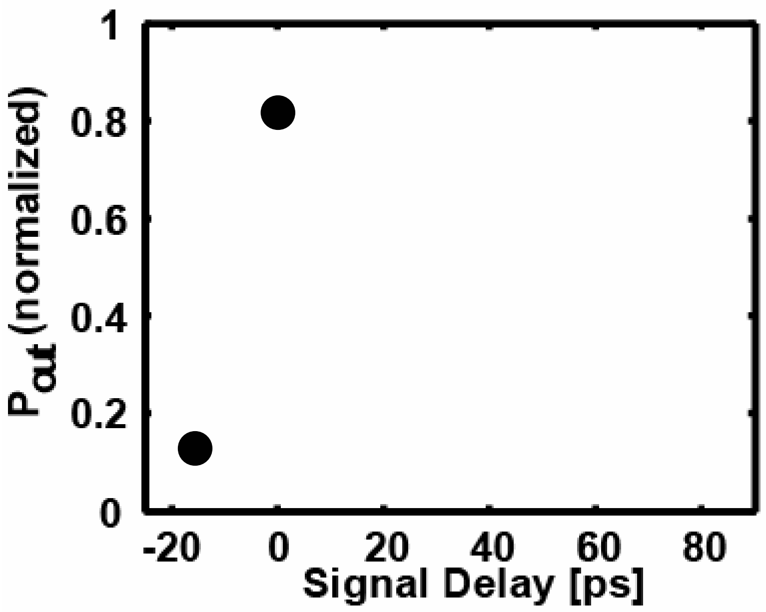

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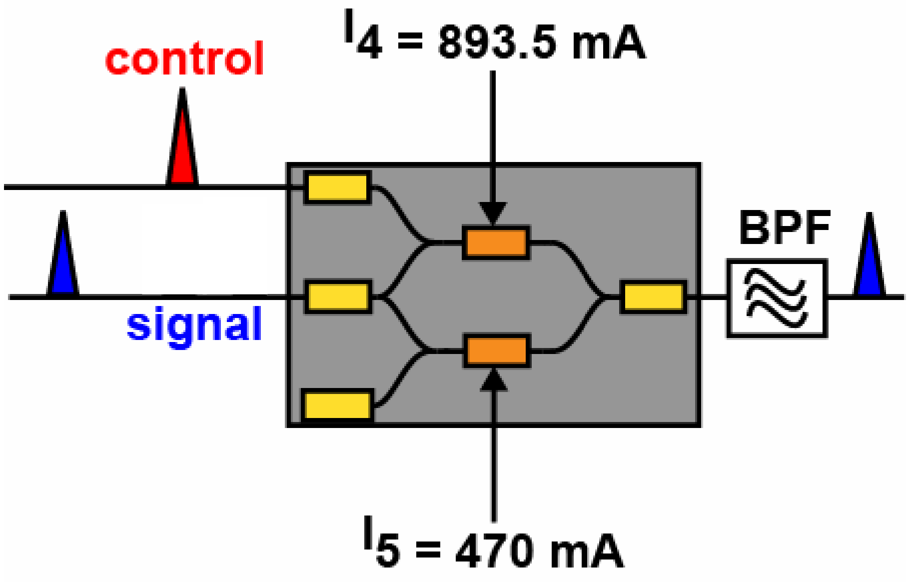
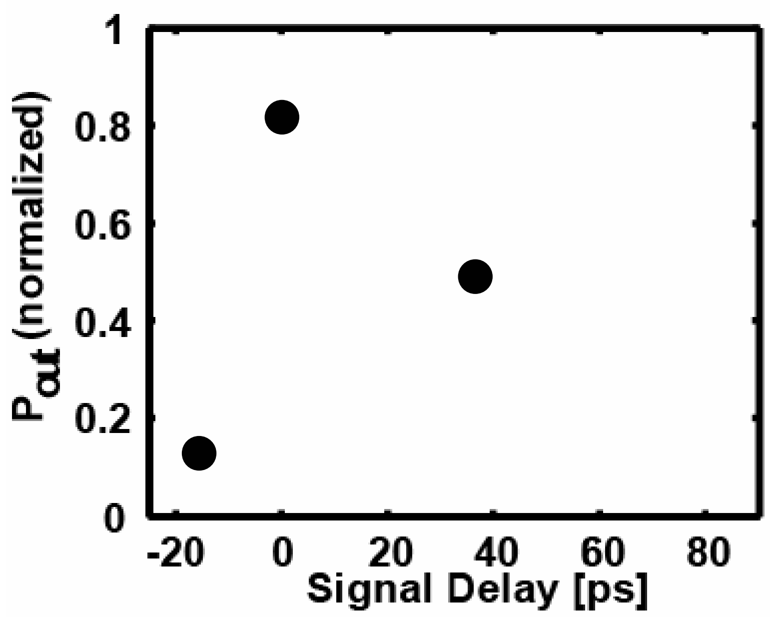
MIT Lincoln Laboratory

Switching Window Measurement





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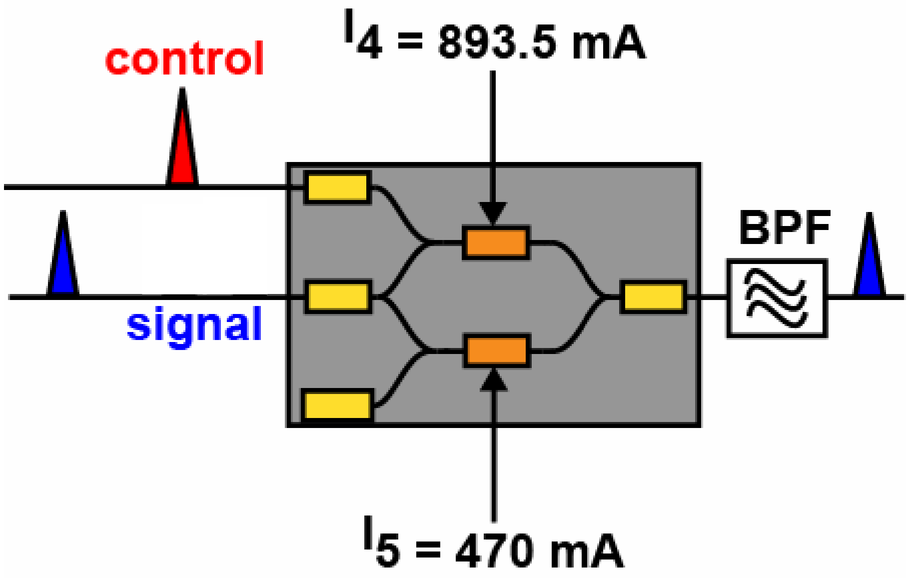
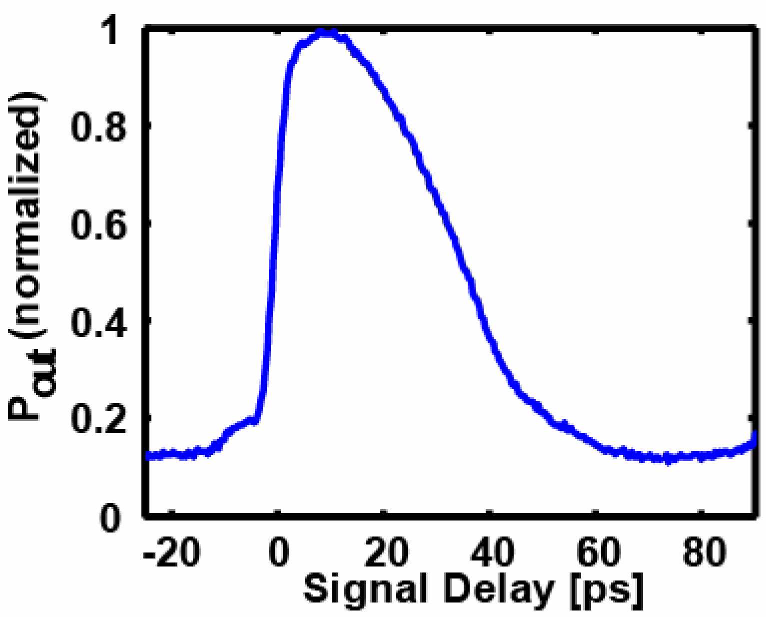
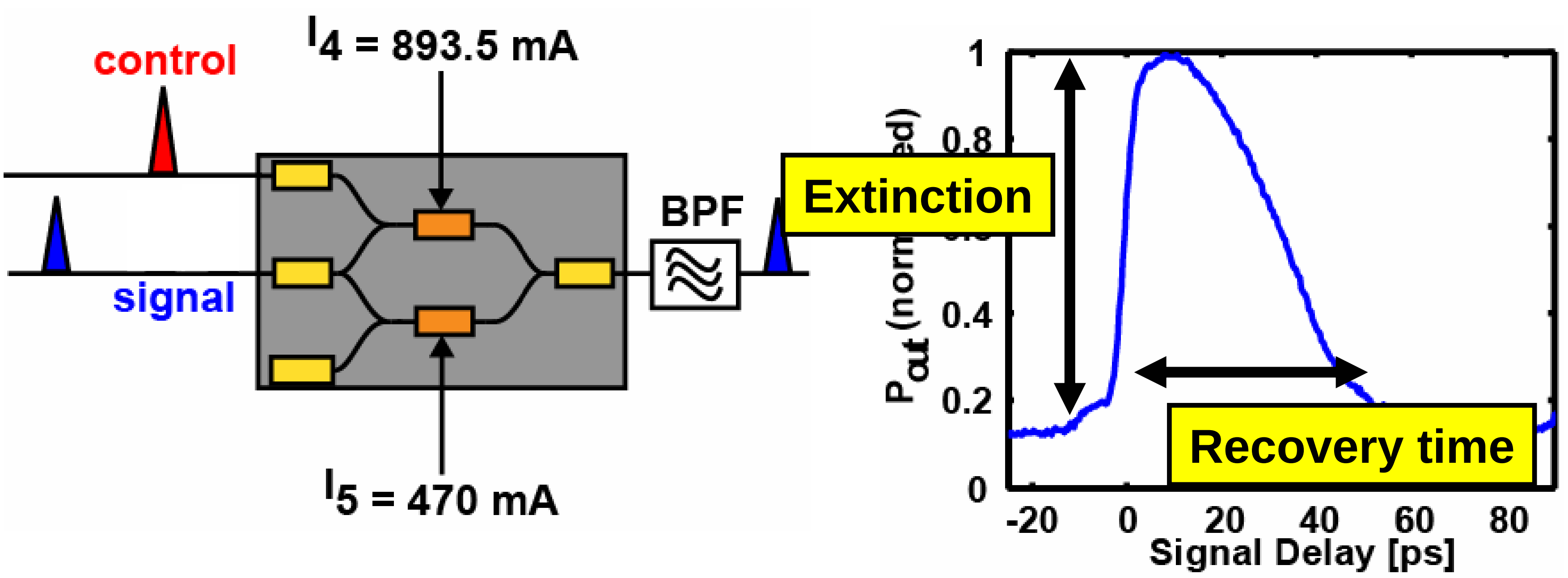




- Fix current bias (I_4, I_5)
- Measure average output power at every control-signal delay
- Continuous measurement can be obtained using a difference-frequency technique

B. Robinson, MIT PhD Thesis, 2003

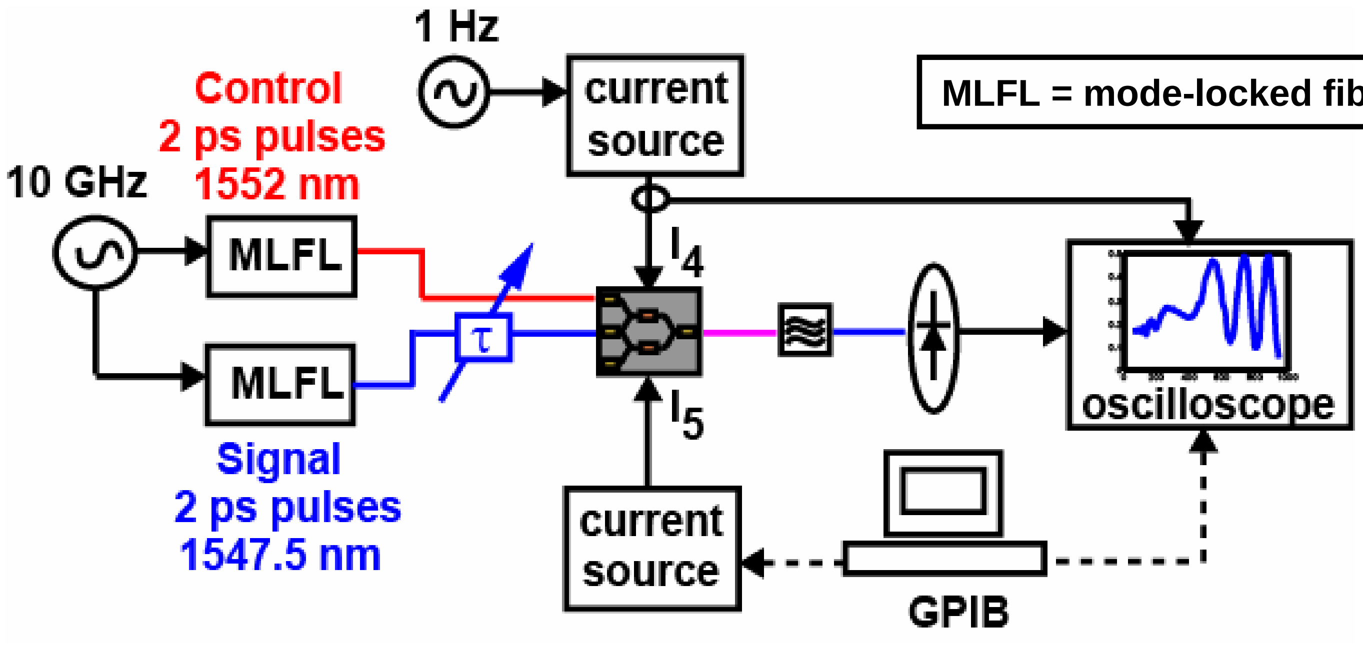
Switching Window Measurement



- Fix current bias (I_4, I_5)
- Measure average output power at every control-signal delay
- Continuous measurement can be obtained using a difference-frequency technique
- Switching dynamics
  - Extinction, Recovery time

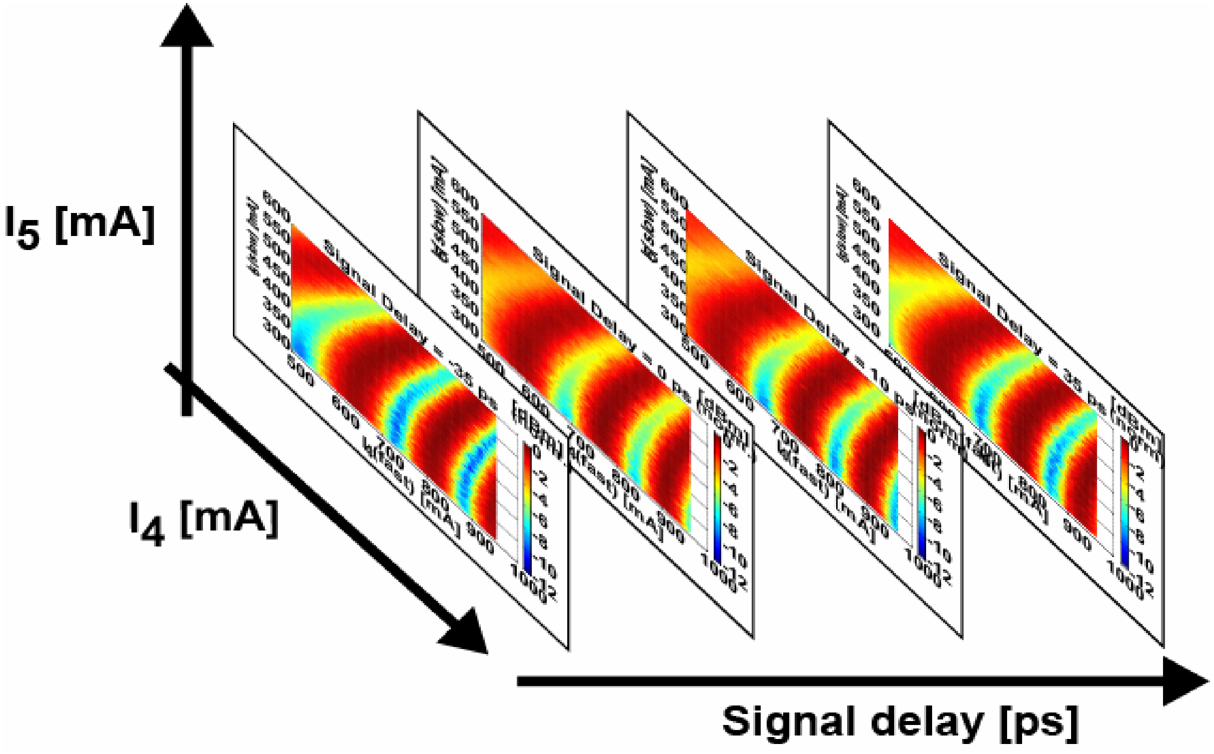
B. Robinson, MIT PhD Thesis, 2003

Combined Measurement: Dynamic Bias Scan



- Simultaneous pump-probe measurement at all bias points
  - At each signal delay, measure a bias map

Dynamic Pump-Probe Bias Scan

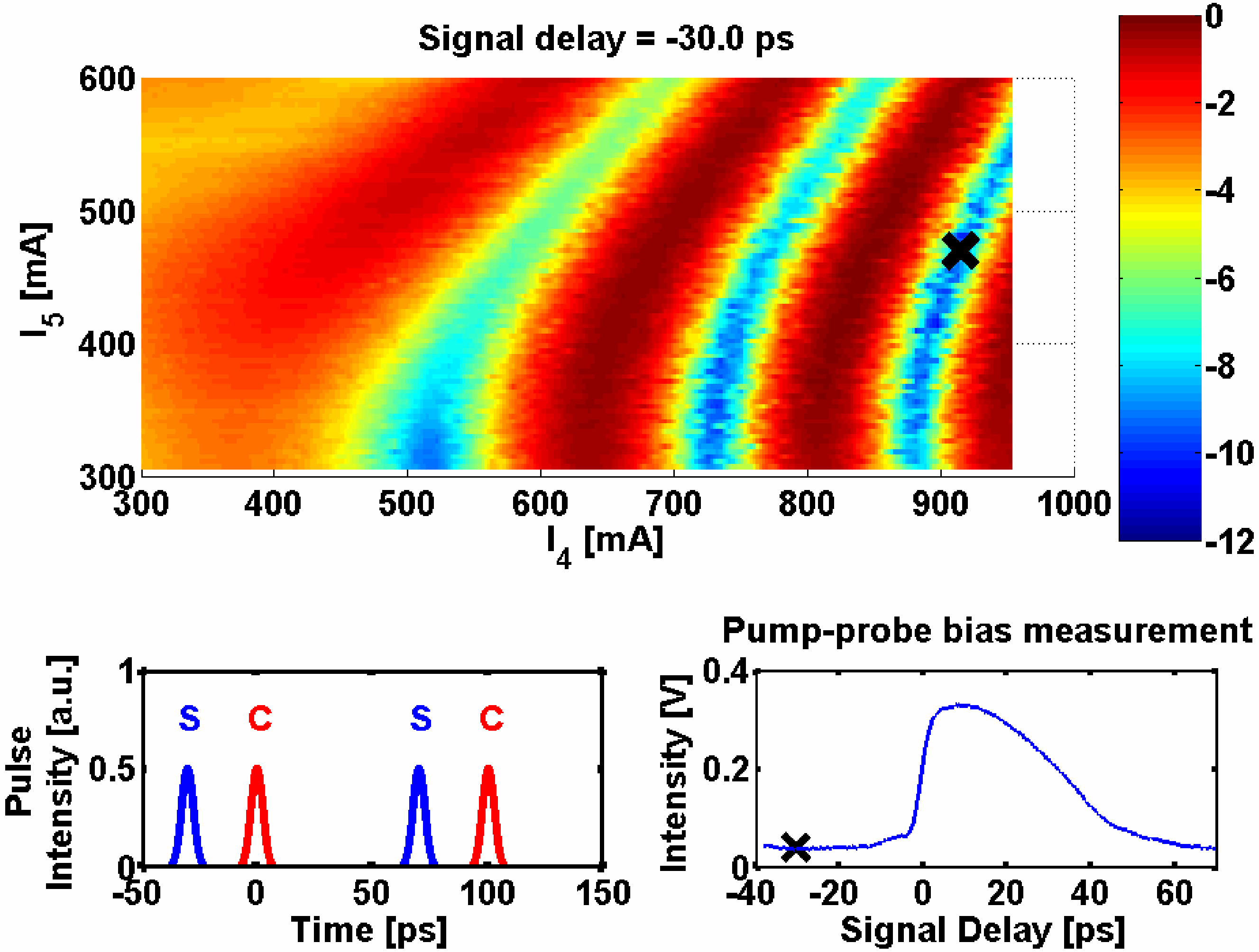


- **Simultaneous pump-probe measurement at all bias points**
  - **At each signal delay, measure a bias map**

- **Measures the effect of optical control pulse on interferometer bias at all operating points: 4-dimensional plot**

J. Wang et al., “A Performance Optimization Method for SOA-MZI Devices”, OFC 2007.

Dynamic Bias Scan

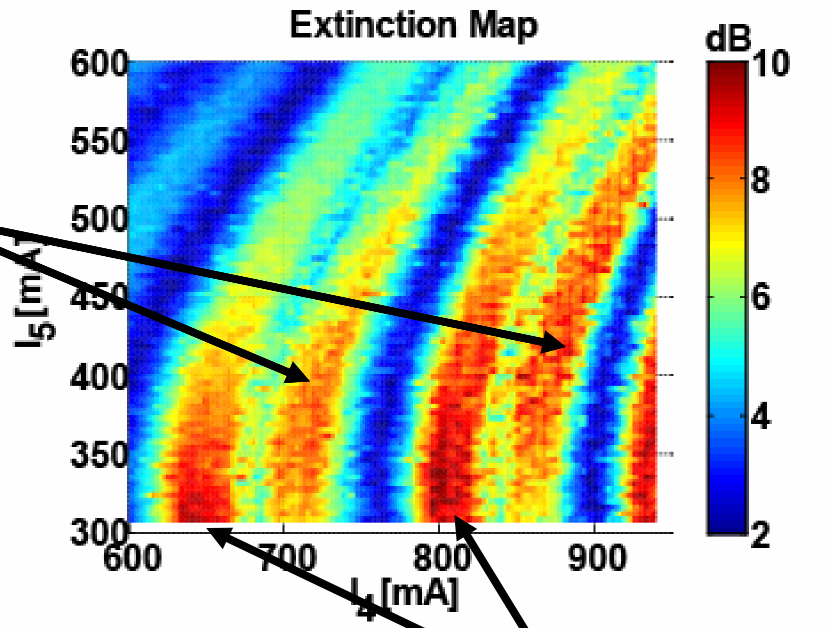


J. Wang et al., “A Performance Optimization Method for SOA-MZI Devices”, OFC 2007.

Extinction Map

- Extinction map: Extract extinction measurement from dynamic bias scan
- Inverting mode gives higher extinction, but logic functions often require non-inverting operation

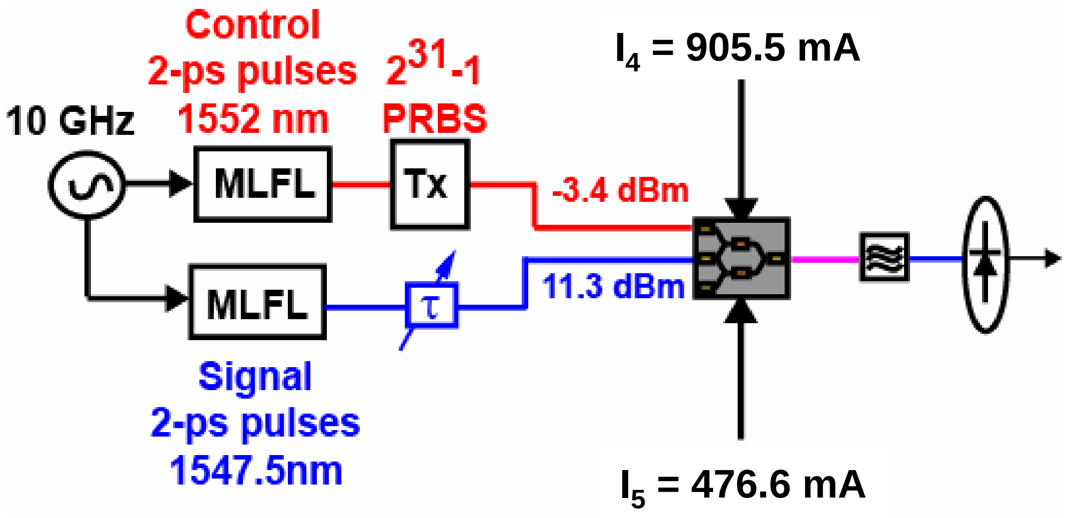
Non-inverting operation

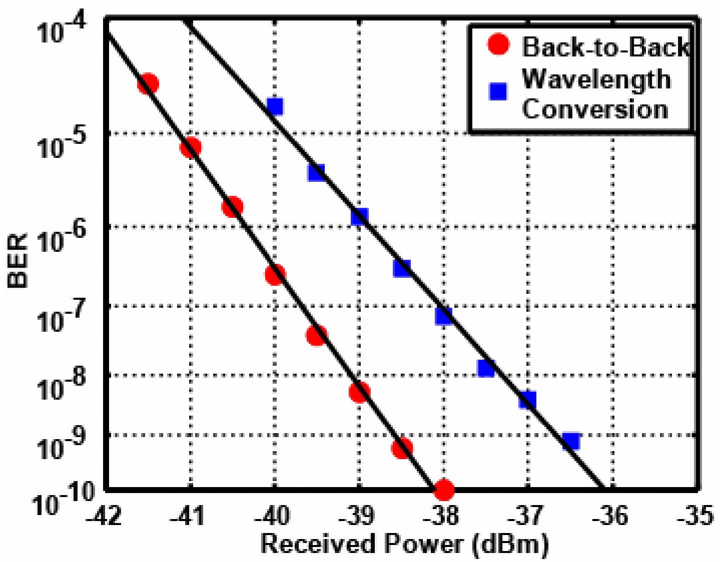


Inverting operation

Wavelength Conversion at Selected Operating Point

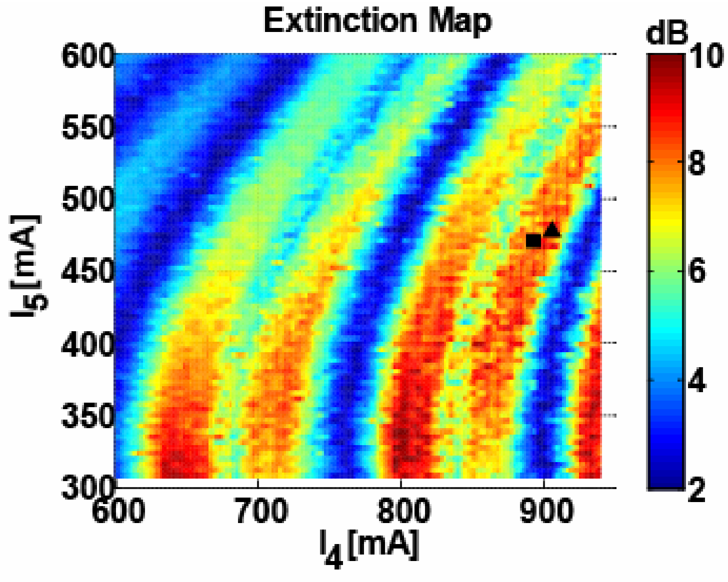
- **Demonstration of effectiveness of dynamic bias map: wavelength conversion**

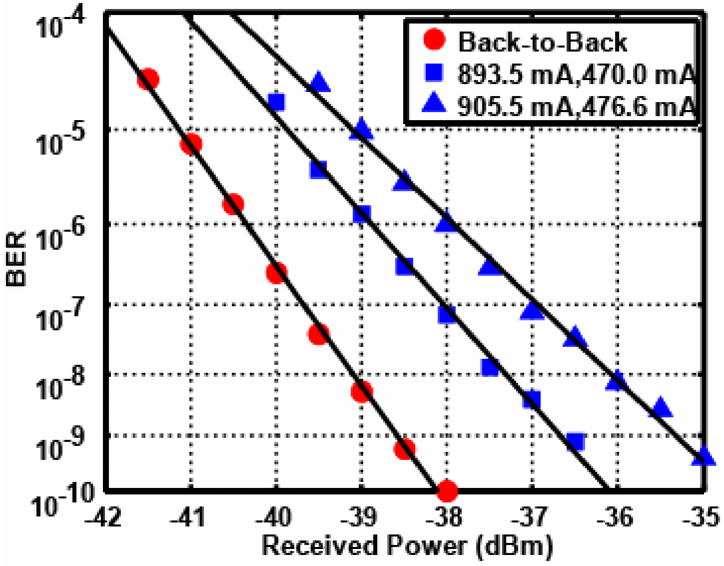




Wavelength Conversion at Selected Operating Point

- Demonstration of effectiveness of dynamic bias map: wavelength conversion
- Compare with nearby operating point found by typical manual optimization





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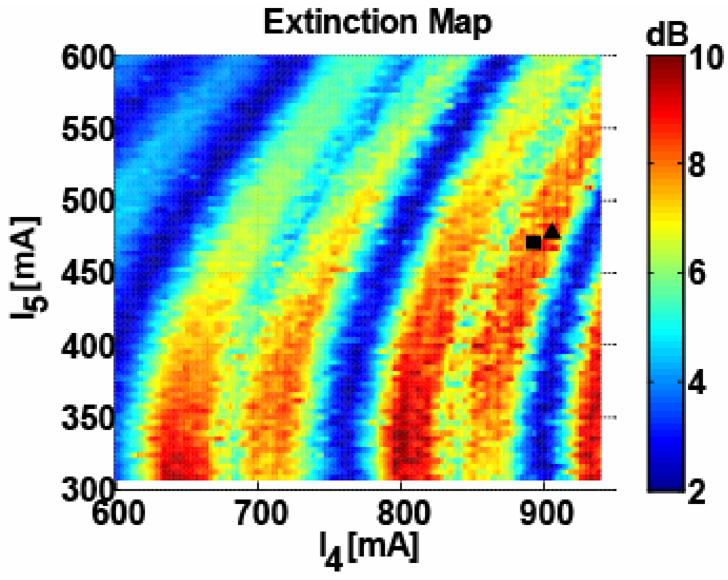
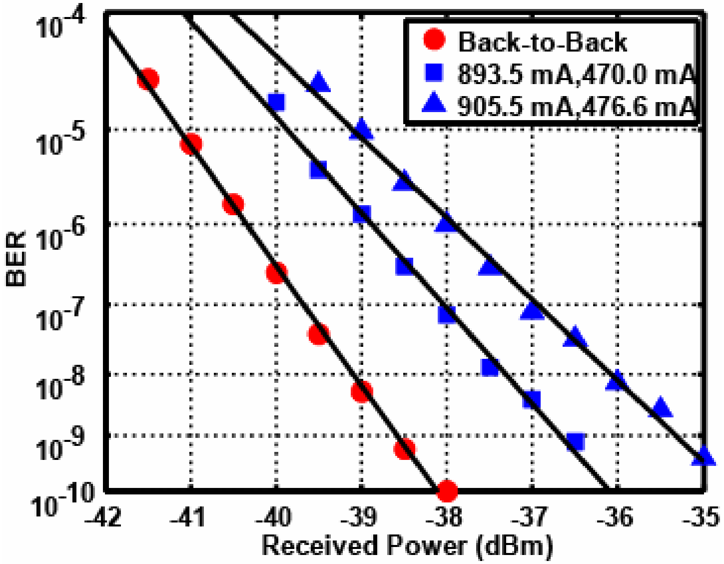




Achievements:

- Highly accurate characterization technique for optimization of ultrafast switch performance
- Improves practical, multi-gate functionality of integrated optical logic

J. Wang et al., “Efficient performance optimization for SOA-MZI devices”, Optics Express 16 (5), 2008.

Outline

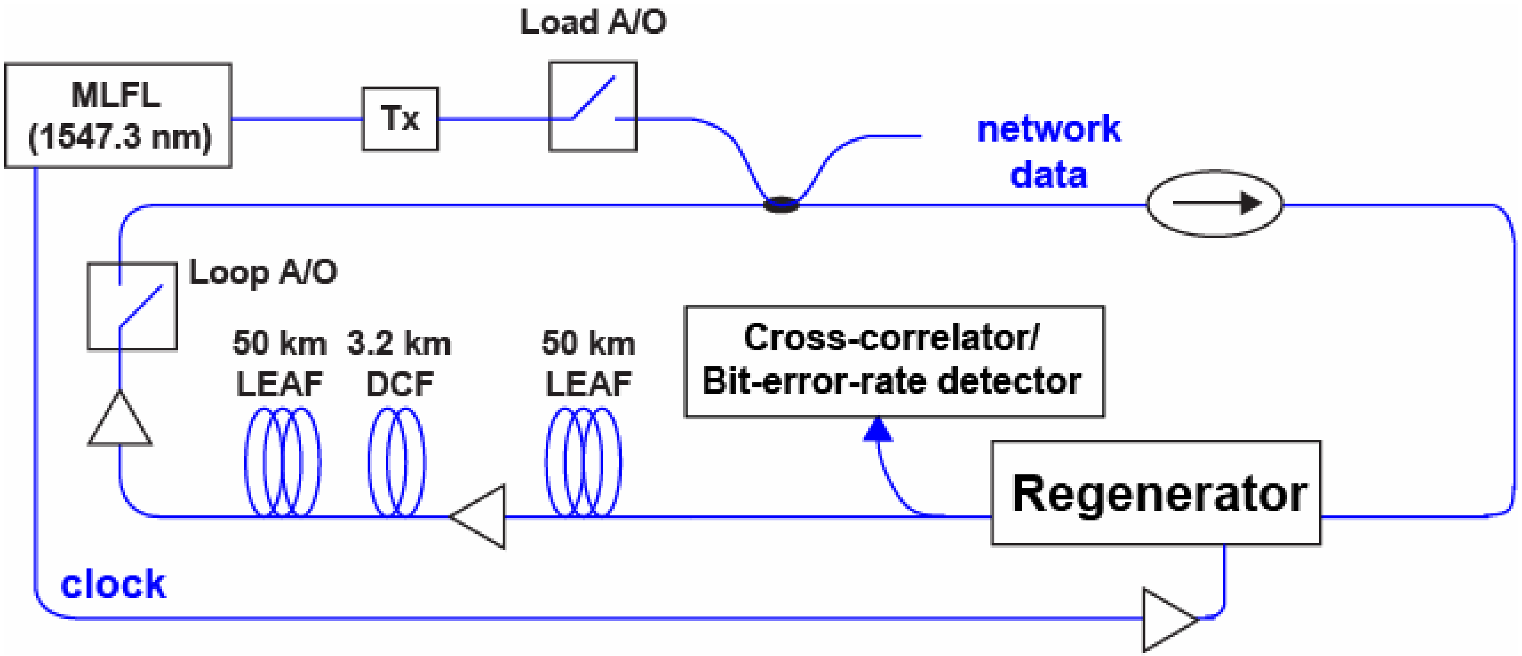
- Motivation/Background
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
- Performance optimization of optical logic gates
- **Regeneration**
- Future SOA-MZI gates
- Conclusion

10,000-km, 100-pass All-Optical Regeneration

- Goal: Demonstrate all-optical error-free regeneration with the SOA-MZI logic gate
- Previous work*:
  - Error-free regeneration with paired SOA-MZI logic gates (inverting operation)
- This work:
  - Wavelength-maintaining regenerator
  - Non-inverting operation (requires only a single logic gate)
  - Polarization insensitive

* Z. Zhu et al., IEEE Photonics Technology Letters 18 (5), 2006.

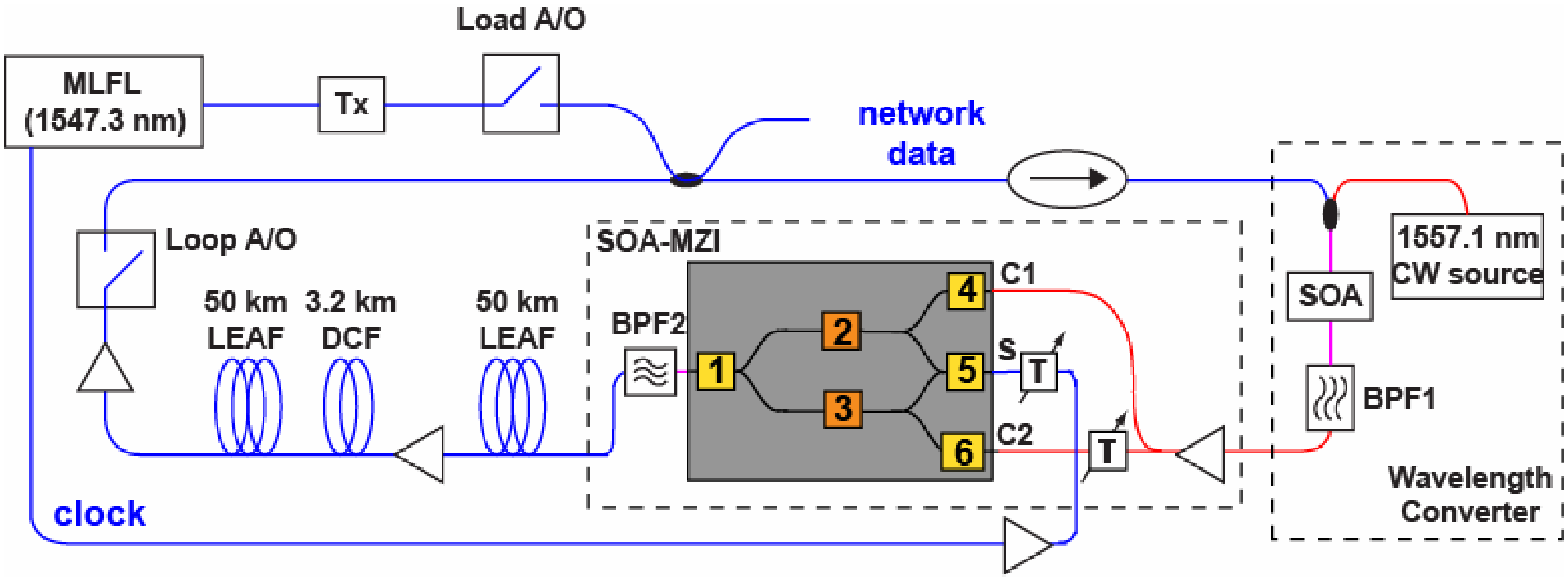
100-km Recirculating Loop Experiment



- **Simulates regenerator performance in real-world system**
- **Tests SOA-MZI in cascading operation**
- **Dispersion compensation cancels 2nd order dispersion**
- **10 Gb/s, 2^{31}-1 pseudo-random bit sequence**

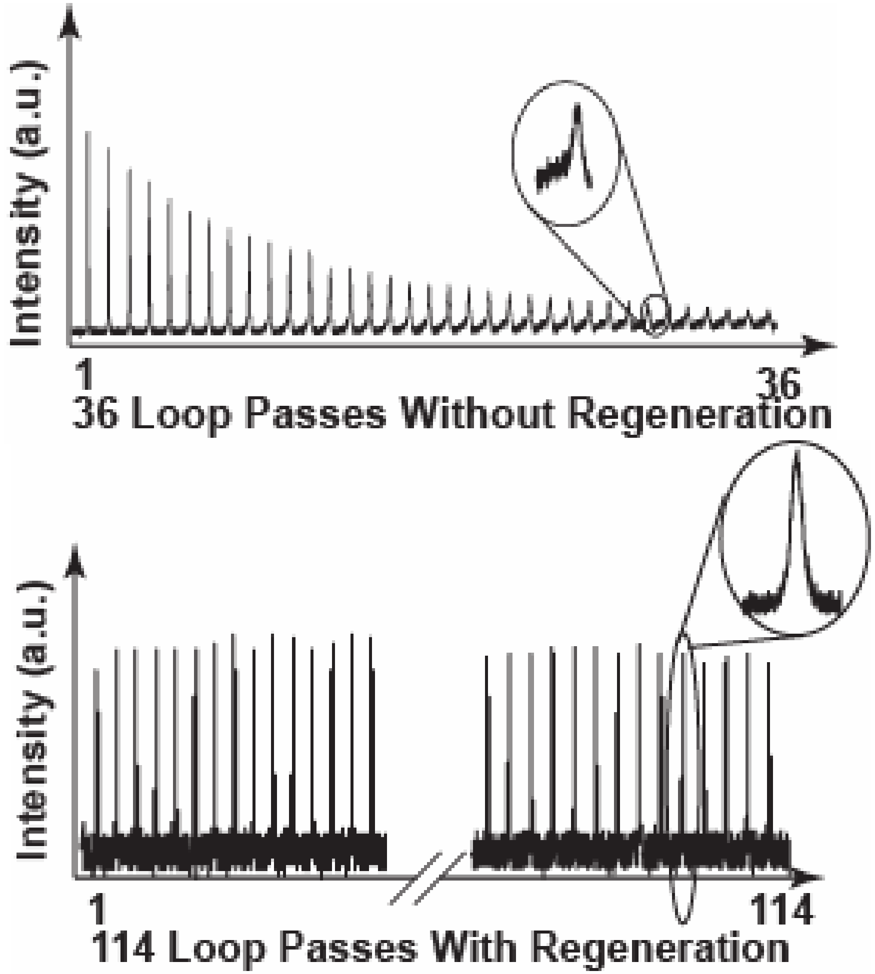
S. J. Savage, "200-pass Picosecond Pulse Transmission through a Regenerative Recirculating Fiber Loop", CLEO 2006.

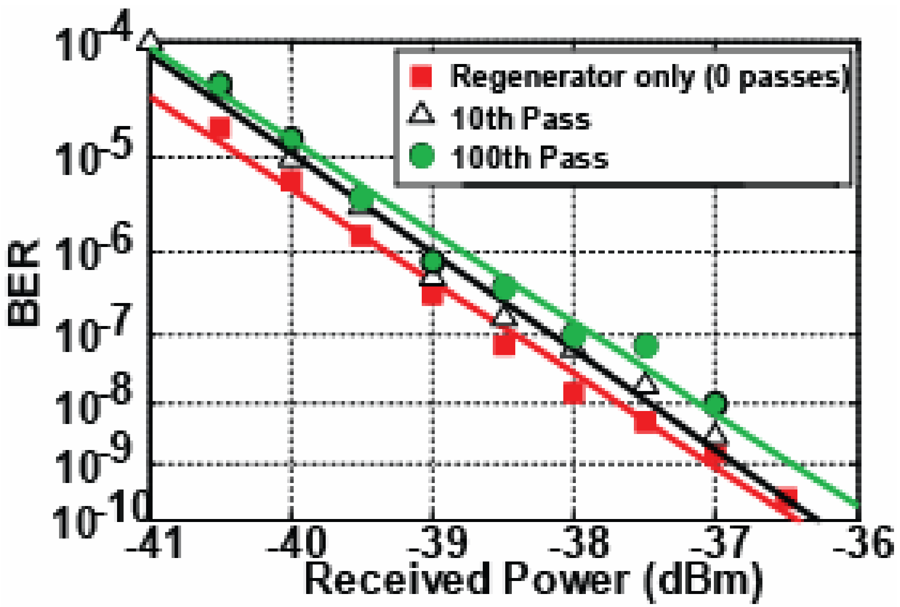
100-km Recirculating Loop Experiment



- Wavelength converter + SOA-MZI = wavelength-maintaining regenerator
- Single SOA-MZI regenerator, non-inverting operation
- Optimal operating point found via dynamic bias map
- Very stable regenerator operation

Regenerator Results: Cross-Correlation and BER





- **Cross-correlation & BER measured after regenerator**
- **0.5-dB penalty after 100 passes (10,000 km)**

J.P. Wang, et al., "Regeneration using an SOA-MZI in a 100-pass 10,000-km Recirculating Fiber Loop," CLEO 2007.

Thus Far...

- Electronic techniques rapidly outgrowing size, weight, power limitations
- Optical signal processing techniques can help:
  - Ultrafast, multi-packet header processing
    - Scalable
    - Low switching energy
    - Network flexibility from payload transparency
    - Reduced O/E/O conversions
  - Practical, easily optimized integrated logic gates
    - Accurate, fast optimization
    - Insight into switching dynamics
  - Cascadable, single-gate wavelength-maintaining regeneration
    - Polarization insensitive
    - Potential for integration
    - 10,000-km, 100 pass demonstration

Outline

- Motivation/Background
- Ultrafast all-optical logic gates
- Routing: 40-Gb/s all-optical header processing
- Performance optimization of optical logic gates
- Regeneration
- **Future SOA-MZI gates: What’s next?**

Integration Platforms

- Hybrid Integration
  - Incompatible materials integrated on a wafer
  - Passive material: silicon, silica
  - Active material: InGaAsP (III-V semiconductors)
  - Challenge: Alignment and fabrication cost

- Monolithic integration
  - Compatible materials grown together for both active and passive devices
  - Challenge:
    - Silicon: active devices
    - InGaAsP: low loss
  - Challenge: high yields

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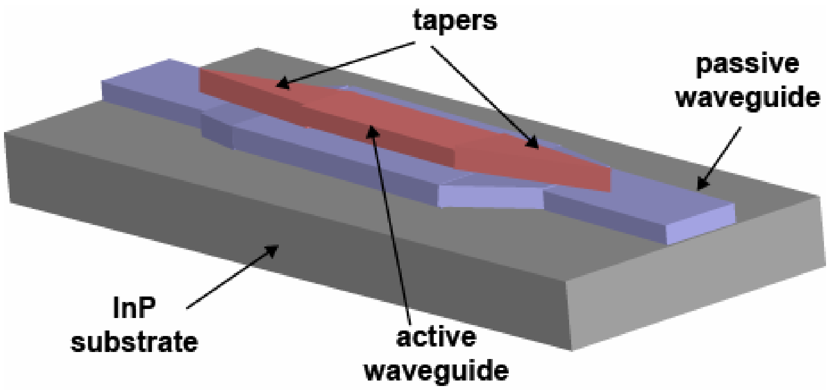
- Asymmetric twin waveguide approach



- Potential for close to 100% coupling
- Potential for high yield
- Tolerance for fabrication errors

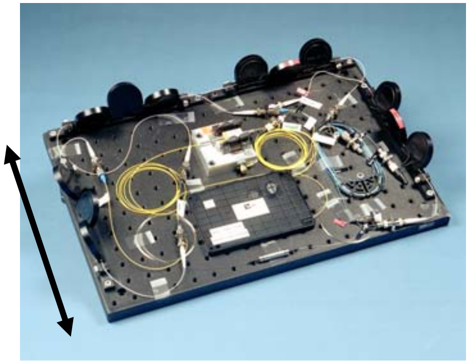
- Collaboration with MIT Integrated Photonics Devices and Materials group

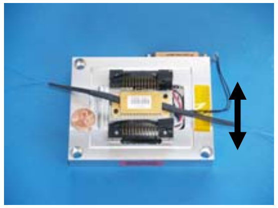
Multi-gate Integrated Optical Logic

- **Previous work:**
  - Simulation and design of SOA-MZI gates (A. Markina)
  - Fabrication of 1st and 2nd generation logic chips (R. Williams)
- **This work:**
  - Characterization of 2nd generation logic chip
  - Recommendations for next generation integrated chips
- **Future work:**
  - Fabrication and design of 3rd generation chips (T. Shih)

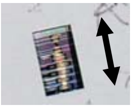
Integration Progress: Size, Power

12”





1”



0.4”

1 logic gate

1 logic gate

Multiple logic gates

Characterization results:

- Demonstrated SOA gain, active/passive coupling
- Loss is currently an issue
- Fabrication improvements will solve these issues

→ **Enable complex logic on a single chip**

Conclusion

- **Demonstrated functionality of all-optical signal processing in routing and regeneration**
  - **40 Gb/s multi-packet header-processing**
  - **10,000-km, 100-pass error free regeneration**
- **Addressed practical implementation of all-optical signal processing**
  - **Developed a simple optimization technique for all-optical logic gate performance**
  - **Demonstrated potential of asymmetric waveguide design for integrated multi-gate logic on a single chip**

Acknowledgements

- Professor Erich Ippen
- Scott Hamilton
- Professor Rajeev Ram

Lincoln Laboratory

- Bryan Robinson
- Shelby Savage
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- Paul Juodawlkis
- Jason Plant
- Reuel Swint
- Todd Ulmer
- Neal Spellmeyer
- Matthew Grein
- Jeffrey Roth
- David Caplan
- Mark Stevens
- Don Boroson
- William Keicher

MIT

- Professor Leslie Kolodziejski
- Gale Petrich
- Ta-Ming Shih
- Ryan Williams (graduated)
- Aleksandra Markina (graduated)
- Tauhid Zaman
- Ali Motamedi
- Reja Amatya

Alphion Corporation

- Boris Stefanov
- Leo Spiekman
- Hongsheng Wang
- Ruomei Mu

Rough Power Comparison

Electronic 3R Regenerator*

- Total power: 10W
- 2 channels
- 2.5 Gb/s per channel
- 40 Gb/s
  - 8 modules
  - 80 W
- 100 Gb/s
  - 20 modules
  - 200 W

But electronic regenerator offers more functionality than just 3R regeneration!

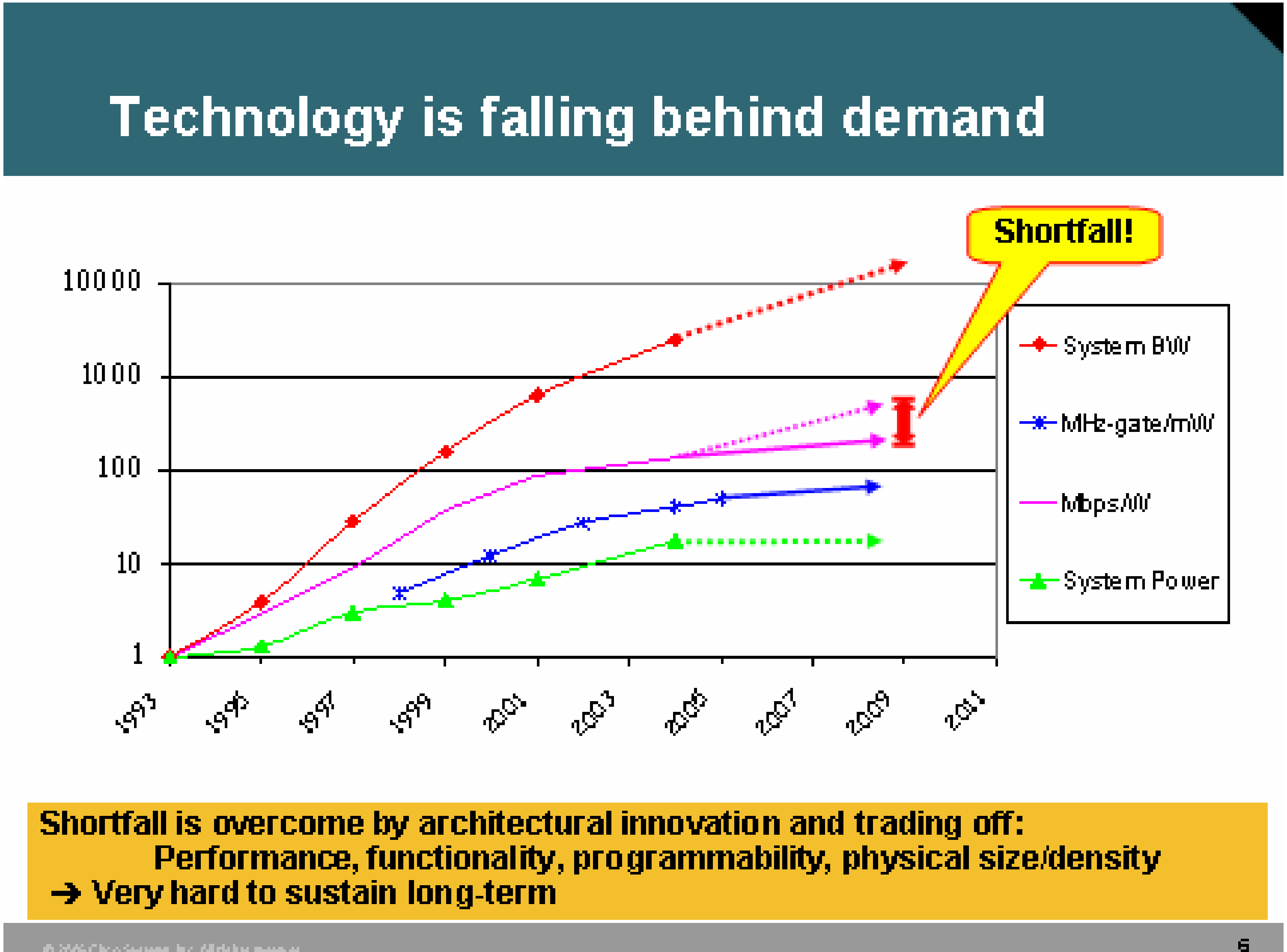
* Cisco WDM Transponder

Optical 3R Regenerator

- 1 optical logic gate
- 1 channel
- Bias power: 600 mW
  - 2 SOAs
  - 200 mA x 1.5 V = 300 mW per SOA
- Switching energy: 40 fJ/bit
  - 40 Gb/s: 1.6 mW
  - 100 Gb/s: 4 mW

  } negligible
- 40 Gb/s
  - 1 switch
  - 600 mW
- 100 Gb/s
  - 1 switch
  - 600 mW

Power Consumption Shortfall

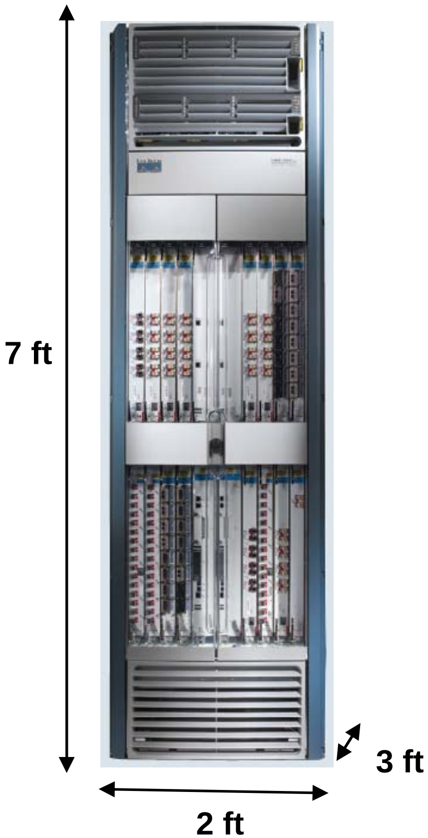


G. Epps, Cisco Routing Research Symposium (2006).

Commercial Electronic Routers

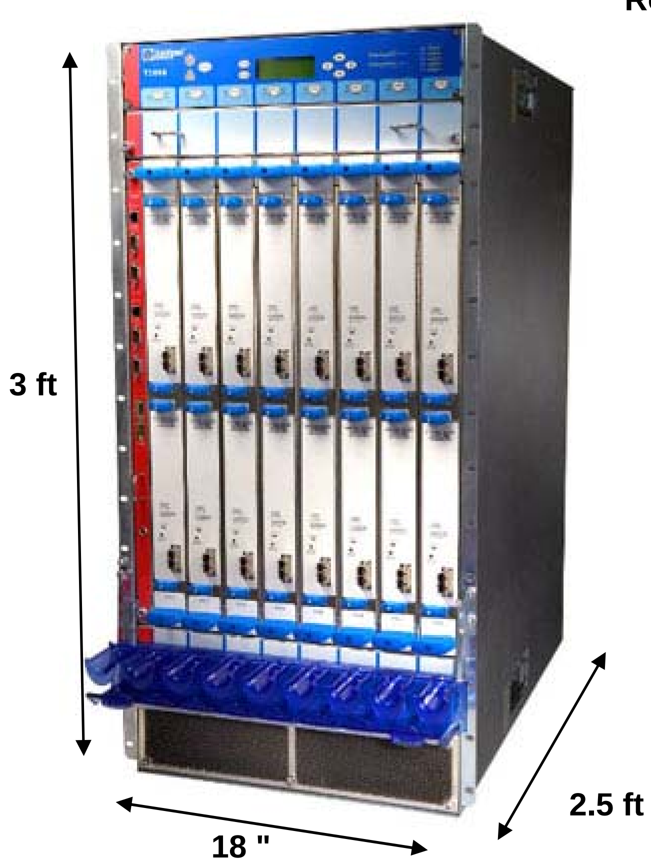
Cisco CSR-1

Throughput: 1.2 Tb/s
Power: 10.9 kW
Weight: 1595 lb.

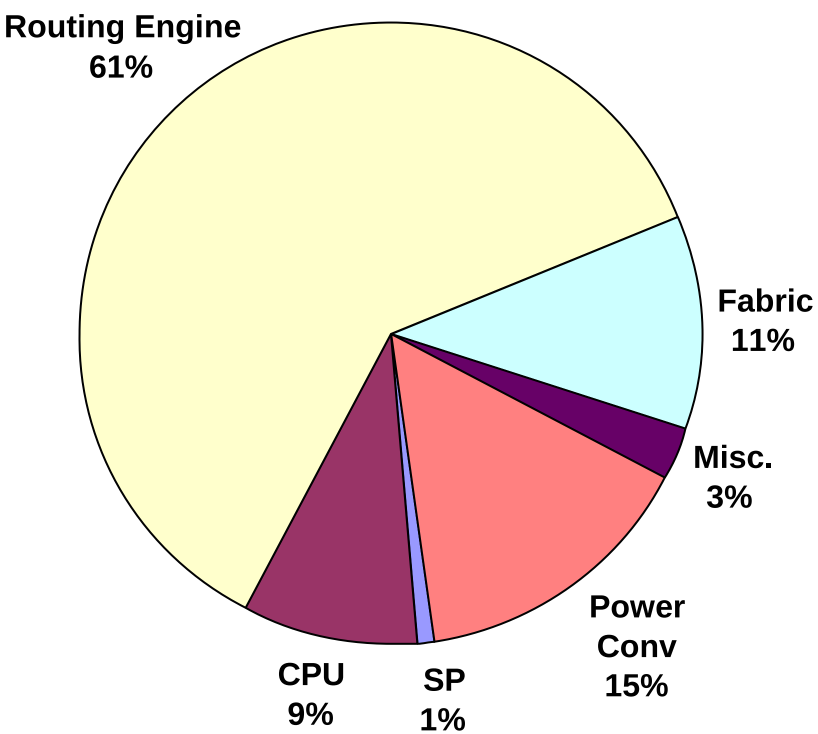


Juniper T1600

Throughput: 1.6 Tb/s
Power: 9.1 kW
Weight: 680 lb.



Power Consumption Allocation by Subsystems* (%)



* Data from G. Epps, Cisco Routing Research Symposium (2006).