FEATURES

- IEEE 802.3 10BaseT and 802.3u 100BaseTx compliant.
- MII interface with serial management.
- Auto negotiation compatible with next page capability.
- 100BaseTx PCS/PMA function with on-chip clock generation and recovery.
- High speed serial front-end logic with minimum transmit and receive latency.
- Built-in 10BaseT ENDEC and transceiver with on-chip waveform shaping and filtering function.
- Current and voltage output for 10BaseT for easy magnetics interface with 100BaseTx PMD.
- Simplified clock requirement with built-in reference clock generation.
- Four programmable LED status display.
- CMOS implementation for low power design.
- 100 pin PQFP package.

GENERAL DESCRIPTION

MTD972 integrates the function of 10BaseT ENDEC and transceiver, 100BaseTx PCS/PMA, and auto negotiation as specified in 802.3u. A Media-Independent-Interface (MII) is used to connect MTD972 with the Media-Access-Control (MAC) layer device. A pseudo-ECL interface from MTD972 is used to connect to external 100BaseTX PMD device, while the on-chip 10BaseT transceiver with built-in waveform shaping and filter function provide the physical layer function for 10BaseT operations.

BLOCK DIAGRAM

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1.0 PIN CONNECTION

100 pin QFP

<table>
<thead>
<tr>
<th>PIN (Name)</th>
<th>Pin#</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_CK</td>
<td>82</td>
<td>O/Z</td>
<td>Transmit clock. This is a continuous clock for timing reference of MII interface. It is 25MHz in 100BaseTx mode, and 2.5MHz in 10BaseT nibble mode, 10MHz in 10BaseT serial mode. It is in high-impedance mode, if MTD972 is put in isolation state.</td>
</tr>
<tr>
<td>TX_EN</td>
<td>74</td>
<td>I</td>
<td>Transmit enable. When TX_EN is set to high, MTD972 enters into transmit state. Data presented on TXD[3:0] is serialized and encoded for transmit. This signal is referenced to the rising edge of TX_CK.</td>
</tr>
<tr>
<td>TX_ER</td>
<td>73</td>
<td>I</td>
<td>Transmit error. When TX_ER is asserted, MTD972 substitute the transmit data with HALT symbol. The assertion of TX_ER has no effect in 10Mb/s operations.</td>
</tr>
<tr>
<td>TXD[3:0]</td>
<td>75, 76, 77, 78</td>
<td>I</td>
<td>Transmit data nibble. This is the transmit data input to MTD972. It is sampled by each TX_CK for data transmission when TX_EN is asserted.</td>
</tr>
<tr>
<td>Name</td>
<td>Pin#</td>
<td>I/O</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>-----</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>RX_CK</td>
<td>62</td>
<td>O/Z</td>
<td><strong>Receive clock.</strong> MTD972 output a continuous clock stream on this pin for receive timing reference. It is 25MHz in 100BaseTx mode, and 2.5MHz in 10Base nibble mode, 10MHz in 10Base serial mode. In 10BaseT mode, RX_CK is locked to the internal generated 20MHz, and transit to the recovered receive clock when receive is active. This output is high impedance state if RX_EN is not asserted or MTD972 is put in isolation state.</td>
</tr>
<tr>
<td>RX_DV</td>
<td>64</td>
<td>O/Z</td>
<td><strong>Receive data valid.</strong> This signal is used to encompass the valid received packet. It is referenced to the rising edge of RX_CK. It is in high impedance if RX_EN is not asserted.</td>
</tr>
<tr>
<td>RX_ER</td>
<td>63</td>
<td>O/Z</td>
<td><strong>Receive error.</strong> This pin is asserted by MTD972 when an error condition occurs during reception of a packet in 100Mb/s operation. Specifically, this include &quot;link fail&quot;, &quot;bad SSD&quot;, and &quot;data error&quot; states. This pin is also used for RXD[5] in bypass modes. This pin has no meaning in the 10Mb/s operation. This pin is put in high-impedance state when RX_EN is not asserted.</td>
</tr>
<tr>
<td>RXD[3:0]</td>
<td>55, 56, 57, 58</td>
<td>O/Z</td>
<td><strong>Receive data nibble.</strong> This is the receive data output from MTD972. It is referenced to the rising edge of RX_CK, and compassed by RX_DV. These pin is in high-impedance state when RX_EN is not asserted.</td>
</tr>
<tr>
<td>RX_EN</td>
<td>43</td>
<td>I</td>
<td><strong>Receive enable.</strong> This pin controls the output enable of RXD[3-0], RX_ER, RX_DV, and RX_CK but not CRS and COL. It has an internal pull-up resistor.</td>
</tr>
<tr>
<td>CRS</td>
<td>66</td>
<td>O/Z</td>
<td><strong>Carrier sense.</strong> This pin is asserted when receive is active, configured in half-duplex mode. It is in high-impedance mode, when MTD972 is in isolation state.</td>
</tr>
<tr>
<td>COL</td>
<td>65</td>
<td>O/Z</td>
<td><strong>Collision.</strong> This pin is used to indicate a collision condition when MTD972 is in half-duplex mode. It also carries the SQE indication in 10Mb/s operation. It is forced low if MTD972 is configured in full-duplex mode. It is in high-impedance mode, when MTD972 is in isolation state.</td>
</tr>
<tr>
<td>MDC</td>
<td>72</td>
<td>I</td>
<td><strong>Management data clock.</strong> This pin should be driven by the management station as the timing reference of MDIO.</td>
</tr>
<tr>
<td>MDIO</td>
<td>67</td>
<td>I/O</td>
<td><strong>Management data input/output.</strong> This is a bi-directional signal between MTD972 and the management station for exchange of control information and data. This pin has an internal pull-up resistor.</td>
</tr>
</tbody>
</table>

**Auto Negotiation**

<table>
<thead>
<tr>
<th>AN2</th>
<th>AN1</th>
<th>AN0</th>
<th>AutoNeg</th>
<th>Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>10Mb/s HDX</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ON</td>
<td>10Mb/s FDX</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ON</td>
<td>100Mb/s HDX</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ON</td>
<td>100Mb/s FDX</td>
</tr>
</tbody>
</table>

*MTD972 Revision 0.7 06/17/1997*
PCS/PMA Control

<table>
<thead>
<tr>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>CRSSEL 47 I</th>
<th>SERMII 98 I</th>
<th>BPALGN 99 I</th>
<th>BP4B5B 100 I</th>
<th>BPSCRM 1 I</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CRS function control. This pin select the function of CRS output. When CRSSEL is high, CRS is asserted only when receive is active regardless of either half or full duplex mode. This pin has an internal pull-down resistor.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Serial control. This pin select the interface method of MII data in 10Mb/s mode. If SERMII is asserted a serial mode is enabled for interfacing with a serial MAC device. Both TX_CK, RX_CK assume 10MHz rate, and data is transferred using TXD[0] and RXD[0]. When not asserted, the transfer assumes MII compliant nibble mode. This pin has no effect in 100Mb/s operation and has an internal pull-down resistor.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Bypass alignment control. This pin is asserted to bypass the 4B/5B coding/encoding, symbol alignment, and scrambling / descrambling process in the 100Mb/s operation. The transmit data in 5 bit format (TX_ER:TXD[3:0]) is serialized and transmitted. The received data also in 5 bit format (RX_ER:RXD[3:0]) is presented on the MII interface. Both TX_CK and RX_CK are still 25MHz. This pin has an internal pull-down resistor.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Bypass 4B/5B code/decode control. Similar to BPALGN, this pin is asserted to bypass the 4B/5B coding/encoding function of MTD972. The MII data interface assumes the 5 bit format. The symbol alignment and scrambling and descrambling function is still effective. This pin has an internal pull-down register.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Bypass scramble / descramble control. Similar to BPALGN, this pin is asserted to bypass the scrambling and descrambling function of MTD972 in 100Mb/s operation. The MII data interface is in nibble format. This pin has an internal pull-down resistor.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Clock Reference

<table>
<thead>
<tr>
<th>CKSEL 14 I</th>
<th>Clock reference mode select. This pin defines the operation modes of reference clock generation and synthesis functions.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKSEL X1 X2</td>
<td>F25MHZ F20MHZ F50MHZ/2 SYN20M X1/X2 OSC</td>
</tr>
<tr>
<td>Pin</td>
<td>Function</td>
</tr>
<tr>
<td>-------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>25M 25M</td>
</tr>
<tr>
<td>1</td>
<td>25M 25M</td>
</tr>
<tr>
<td>X1/X2</td>
<td>X1/X2 OSC SYN20M</td>
</tr>
<tr>
<td></td>
<td>If CKSEL=F, MTD972 output the divided by half signal from F50MHz to F25MHz for internal reference. If X1 is forced to hard high, than 20MHz is synthesized. If X1 and X2 is connected to a 20MHz crystal oscillator, the oscillator output is used for internal reference. If CKSEL=1 or 0, MTD972 uses X1 and X2 on-chip oscillator for 25MHz generation, and synthesizes the internal 20MHz. In this case, a 25MHz crystal should be connected between X1 and X2.</td>
</tr>
<tr>
<td></td>
<td><strong>REFIN</strong> 86 I 25MHz reference clock in. All internal timing is derived from the clock input of this pin. A 25MHz continuous clock should be connected to this pin. The clock source can be an external oscillator, or the output of F25MHZ.</td>
</tr>
<tr>
<td>2</td>
<td>25MHz reference clock in. All internal timing is derived from the clock input of this pin. A 25MHz continuous clock should be connected to this pin. The clock source can be an external oscillator, or the output of F25MHZ.</td>
</tr>
<tr>
<td></td>
<td><strong>F50MHZ</strong> 2 I 50MHz reference clock in. A 50MHz clock signal can be applied to this pin to generate 25MHz clock at F25MHZ output for internal reference. If not used, this pin should be pulled low. It has an internal pull-down resistor.</td>
</tr>
<tr>
<td></td>
<td><strong>X1</strong> 33 I Crystal oscillator. The output of on-chip crystal oscillator. It can be used to generate either 25MHz or 20MHz clock depending on the CKSEL selection. If an external clock is used, it should be applied to this pin. If it is forced high (to VDD or pull-up by a resistor less than 4.7K), the oscillator is disabled, and internal synthesized clock is used.</td>
</tr>
<tr>
<td></td>
<td><strong>X2</strong> 34 I Crystal oscillator. The input of on-chip crystal oscillator. If an external clock is used to applied at X1, X2 should be left open.</td>
</tr>
<tr>
<td></td>
<td><strong>F25MHZ</strong> 81 O/Z 25MHz reference clock out. This pin output a 25MHz continuous clock from either divided by 2 of 50MHz input, or the 25MHz clock of on-chip oscillator.</td>
</tr>
<tr>
<td></td>
<td><strong>F20MHZ</strong> 83 O/Z 20MHz reference clock out. This pin output a 20MHz continuous clock from either the 20MHz on-chip oscillator, or the synthesized 20MHz. This pin default in high-impedance mode after reset.</td>
</tr>
<tr>
<td></td>
<td><strong>10BaseT PMD</strong></td>
</tr>
<tr>
<td></td>
<td><strong>TPIP, TPIN</strong> 20, 21 I Differential twisted-pair receive input. A differential UTP receive signal for 10Mb/s is input from these two pins. The inputs are internally biased at 1/2 Vdd.</td>
</tr>
<tr>
<td></td>
<td><strong>TPOVP, TPOVN</strong> 25, 26 O Differential voltage mode twisted-pair transmit output. These two pins provide a voltage mode output for 10Mb/s UTP transmit data. A serial termination resistor of 10.5Ohm should be connected between each pin to the transformer. The isolation transformer should have turn ratio of 1:2. The idle voltage on these two pins are at 2/3 Vdd.</td>
</tr>
<tr>
<td></td>
<td><strong>TPOIP, TPOIN</strong> 23, 24 O Differential current mode twisted-pair transmit output. These two pins provide a current source mode output for 10Mb/s UTP transmit data. Each pin should have a 50 Ohm termination resistor connected to Vdd while connecting to the isolation transformer. The transformer should have turn ration of 1:1 with center-tap in the primary side connected to Vdd.</td>
</tr>
<tr>
<td></td>
<td><strong>OVISEL</strong> 29 I Output voltage/current mode select. This pin controls the power-on default setting of 10BaseT PMD output mode. If this pin is low, the voltage output, TPOVP, and TPOVN are enabled. If this pin is pulled high, TPOIP and TPOIN, current mode output is enabled.</td>
</tr>
</tbody>
</table>
### 100BaseT PMD

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDP, RDN</td>
<td>5, 6</td>
<td><strong>Differential pseudo-ECL receive input.</strong> A differential pseudo-ECL level receive signal from the 100 Mb/s PMD should be applied to these inputs.</td>
</tr>
<tr>
<td>SDP, SDN</td>
<td>7, 8</td>
<td><strong>Differential pseudo-ECL signal-detect input.</strong> A differential pseudo-ECL level signal detect status from the 100 Mb/s PMD should be applied to these inputs.</td>
</tr>
<tr>
<td>TDP, TDN</td>
<td>16, 17</td>
<td><strong>Differential pseudo-ECL transmit output.</strong> A differential pseudo-ECL level transmit output to the 100 Mb/s PMD is presented on these pins. Both outputs are source follower type and proper external ECL loads are required.</td>
</tr>
</tbody>
</table>

### PMD Control

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>100BTX</td>
<td>89</td>
<td><strong>100BaseTx media status.</strong> This pin is asserted high when MTD972 is in 100Mb/s operation.</td>
</tr>
<tr>
<td>10BAST</td>
<td>54</td>
<td><strong>10BaseT media status.</strong> This pin is asserted high when MTD972 is in 10Mb/s operation.</td>
</tr>
<tr>
<td>ENCSEL</td>
<td>53</td>
<td><strong>Encode select for 100BaseTx PMD.</strong> This pin reflects the value of PCR[11].</td>
</tr>
<tr>
<td>LBKN</td>
<td>49</td>
<td><strong>Loopback control for 100BaseTx PMD.</strong> This pin is asserted low when LBCR[9:8] assumes the value of 01 indicating a PMD loopback function. This pin should be connected to the loopback control of PMD device.</td>
</tr>
</tbody>
</table>

### LED Status Output

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEDT</td>
<td>42</td>
<td><strong>Transmit LED.</strong> This pin is driven low when MTD972’s transmit is active.</td>
</tr>
<tr>
<td>LEDR</td>
<td>41</td>
<td><strong>Receive LED.</strong> This pin is driven low when MTD972’s receive is active.</td>
</tr>
<tr>
<td>LEDL</td>
<td>38</td>
<td><strong>Link status LED.</strong> This pin is driven low when MTD972 detect a link good status from either 10Mb/s or 100Mb/s PMD.</td>
</tr>
<tr>
<td>LEDP</td>
<td>37</td>
<td><strong>Polarity/Duplex LED.</strong> This pin is driven low when a normal polarity is detected in 10Mb/s PMD or full-duplex operation is selected.</td>
</tr>
<tr>
<td>LEDC</td>
<td>36</td>
<td><strong>Collision LED.</strong> This pin is driven low when a collision condition occurs. It is deasserted in full-duplex operation.</td>
</tr>
</tbody>
</table>

### PHY Address (These input are shared)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA0</td>
<td>49</td>
<td><strong>Shared with LBKN.</strong> The value of this pin is latched by MTD972 during reset to determine the PHY address.</td>
</tr>
<tr>
<td>PA1</td>
<td>53</td>
<td><strong>Shared with ENCSEL.</strong> The value of this pin is latched by MTD972 during reset to determine the PHY address.</td>
</tr>
<tr>
<td>PA2</td>
<td>66</td>
<td><strong>Shared with CRS.</strong> The value of this pin is latched by MTD972 during reset to determine the PHY address.</td>
</tr>
<tr>
<td>PA3</td>
<td>89</td>
<td><strong>Shared with 100BTX.</strong> The value of this pin is latched by MTD972 during reset to determine the PHY address.</td>
</tr>
<tr>
<td>PA4</td>
<td>63</td>
<td><strong>Shared with RX_ER.</strong> The value of this pin is latched by MTD972 during reset to determine the PHY address.</td>
</tr>
</tbody>
</table>

### Misc.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mode</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>44</td>
<td><strong>External reset.</strong> Asserting this pin cause a hardware reset in MTD972’s internal circuits.</td>
</tr>
<tr>
<td>TESTPCS</td>
<td>48</td>
<td><strong>Test mode selection for PCS logic.</strong> Asserting this pin enables PCS test mode. This pin has internal pull-down resistor.</td>
</tr>
</tbody>
</table>
### 3.0 FUNCTIONAL DESCRIPTIONS

#### 3.1. Reset logic

MTD972 has an internal power-on detector that maintains the reset condition if Vdd is less than 4.0V. After Vdd is greater than 4.0V, the reset condition is extended by 4 msec. The internal reset is the OR of power-on reset and the external reset (RESET) pin. Note that the external reset is not extended.

#### 3.2. Clock reference

MTD972 uses both 25MHz and 20MHz as reference timing internally. To facilitate flexible clock distribution on system level, various clocking scheme can be used for MTD972.

If CKSEL is left floating, then MTD972 assumes an external 25MHz source to be applied at REFIN pin. If the system has a 50MHz clock, then it should be connected to the F50MHZ input of MTD972, and a divided by 2 25MHz is generated on the F25MHZ output. Thus one can connect F25MHZ to REFIN. Or if the system has 25MHz clock, the system clock can be connected directly to REFIN. The 20MHz can be generated by connecting a crystal to X1, X2 pins. Or by tying X1 to HIGH, MTD972 uses the 25MHz to synthesize the 20MHz and provide a continuous 20MHz clock on F20MHZ output.

If CKSEL is forced LOW, MTD972 assumes a 25MHz crystal is connected across X1 and X2. F25MHZ is the output of the on-chip oscillator. One then should connect F25MHZ to REFIN for internal reference. In this case, MTD972 always synthesizes the 20MHz.

Other implementations of system clocking schemes are possible, the operation of MTD972 is tabulated in the following table. REFIN should have a 25MHz continuous clock applied for proper operations.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>X1</th>
<th>X2</th>
<th>F25MHZ</th>
<th>F20MHZ</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25M</td>
<td>25M</td>
<td>X1/X2 OSC</td>
<td>SYN20M</td>
</tr>
<tr>
<td>1</td>
<td>25M</td>
<td>25M</td>
<td>X1/X2 OSC</td>
<td>SYN20M</td>
</tr>
<tr>
<td>20M</td>
<td>0/F</td>
<td>0/F</td>
<td>F50MHZ/2</td>
<td>SYN20M</td>
</tr>
<tr>
<td>20M</td>
<td>0/F</td>
<td>0/F</td>
<td>F50MHZ/2</td>
<td>X1/X2 OSC, SYN20M</td>
</tr>
</tbody>
</table>

#### 3.3 Clock Generation Module (CGM)

An internal frequency multiplier block is used to synthesize a 125 MHz transmit bit clock from the REFIN reference clock for 100 Mbps operation. The CGM also generate a 20 MHz clock for the 10 Mbps function. The synthesizer is implemented in a precision PLL with on-chip loop filter to provide low jitter timing reference.
CGM also include the function of 100Mbps transmit. The serial transmit data in NRZI format is sampled by the transmit bit clock. A differential pseudo-ECL driver is used to drive TDP and TDN output pins.

3.4 Clock Recovery Module (CRM)
The CRM is used to provide an accurate synchronization for the 100 Mbps received data. A reference 125 MHz clock from CGM is used for a timing reference in the CRM. The synchronization to the incoming data stream is achieved by aligning the delay of the reference clock to the data edge.

CRM also include the function of data slicing. Data sampling is achieved by a fast data comparator with the synchronized received bit clock.

3.5 100Mb/s Function
3.5.1 Transmit

The nibble data from MII interface first go through 4B/5B symbol encoder at 25MHz rate. The transmit function is controlled by the PCS transmit state machine. The 5B data is then converted to 125MHz serial form and fed into the scrambler. A serial scrambler running at 125MHz is used to achieve minimum...
transmit latency. The output of the scrambler is then converted to NRZI format at the PMA-TX functional block. 100Base-X transmitter consists of function blocks, which convert synchronous 4B data to 5B data, scramble 5B data, and change it to be 125Mb/s serial data stream.

1. Symbol Encoder
The symbol encoder converts 4B nibble data to 5B symbol. This conversion allow control symbol to be transmitting along with data stream. At the beginning of the packet, the encoder will replace the first byte of preamble with J/K symbol denote the beginning of a packet. And add T/R at the end. Between the gap of two packet, add idle symbol.

2. Scrambler
The scramble is used to suppers the radiated emissions at the connector and twisted pair. The scrambler use 11 bits LFSR to combine 5B code via XOR gate.

3. NRZI encoder
Encode NRZ to NRZI for 802.3u specification.

3.5.2 Receive

Figure 2. 100Mbps receive data flow
The serial received data from RDP and RDN pins are sampled by the CRM. The output of the receive front end is first converted from NRZI format to NRZ format and then fed into a serial descrambler. The use of serial descrambler running at 125MHz ensures minimum receive latency in the receive data path. Output of the descrambler is sent to the 5B/4B decoder controlled by the PCS receive state machine. The 100Base-X receiver recover the data and clock from input data pair. Then decode and align to be 4b nibble data.

1. NRZI decoder
Before descramble, must decode data to be NRZ format.

2. Descrambler
To descramble input data, the descrambler must generate identical key to recover the original data. In order to maintain the synchronization of the key, the descrambler monitor the descrambled data for each 722 us. If there is not sufficient idle pattern, it will do synchronize again.

3. Symbol decoder
After detect the start pattern "J/K", the symbol alignment will begin, and will change the phase of RX_CK. The symbol decoder acts as a look up table convert 5B code to 4B data.

3.5.3 Carrier Sense and Collision
The carrier sense condition is asserted when either transmit and receive is active in half duplex mode. For full-duplex mode, only receive activity will assert the carrier sense signal. The collision condition is asserted if both transmit and receive are active in half-duplex mode. In full-duplex mode, the collision is always deasserted.

3.5.4 Link Status
The link monitor has a redundant carrier detect function. The link status is determined by the SD input. The link is asserted after a preset time of SD assertion according to the link monitor state diagram of 802.3 24.3.4.4.

The link function also include Far-End-Fault detect and generation. These functions can be optionally enabled or disabled by the control register.

3.6 10Mbps Function
3.6.1 Transmit
The transmit data from MII can take either nibble or serial format. An internal 20MHz reference clock is used to clock the Manchester encoder. The encoded data is sent to the UTP output driver.

Two set of output are available in MTD972. TPOIP and TPOIN are differential current-mode output with built-in waveform shaping function. This output pair can be connected directly to the output of 100MHz PMD device. A 50 Ohm resistor connected to each pin and +5V should be used as a common load among the 10Mbps and 100Mbps PMD. In addition, a 1:1 transformer with center-tap connected to +5V should be used for coupling to UTP media.

TPOVP and TPOVN are differential voltage-mode output also with built-in waveform shaping function. The output is a voltage source with very low output impedance, thus requires a series resistor to connected to the transformer for media coupling. A 1:2 transformer and 12.5 Ohm resistors should be used.

3.6.2 Receive
TPIP and TPIN is the receive differential pair for 10Mbps. These two pins are internally biased. The differential signal need to meet both AC and DC squelch condition to enable the receive data path.
received signal is connected to link test circuit to determine link status.

An on-chip PLL is used for Manchester decoding. The PLL is locked to an internally generated 10MHz clock and acquire fast phase synchronization to the incoming data edge of the preamble of the packet. Decoded data is then formatted to nibble width and passed to MII interface.

3.7 Auto-negotiation
MTD972 implements auto-negotiation logic conforming to the 802.3u specification. The basic operation is based on using FLP to communicate information between link partners. The auto-negotiation takes three phases to complete: advertising, detection and selection.

The auto-negotiation mode can be optionally selected using external pin selection AN[0-2]. MTD972 also implement parallel detect function to allow compatibility with legacy network devices. Next page function is also supported by MTD972 that allows exchange of arbitrary information between link partners, and both message pages and unformatted page format are supported.

3.8 MII Serial Management and Register Access
The MTD972 implement a set of control and status registers which MII specification required, and a subset of option register. The access method is described below.

3.8.1 Serial Management Access Protocol

![Typical MII Read Operation](image)

![Typical MII Write Operation](image)

MII specification defines two pins, MDC and MDIO for serial management. MDC has a maximum clock rate 2.5MHz. MDIO is bi-directional and may be shared up to 32 devices. MDIO required a 4.7k Ohm pull up resistor when idle. Before any transaction, the station must send 32 continuous logic "1" on MDIO to establish synchronization.

Figure 3 shows the read and write operation. The start code is "01" followed by an op code, either "01" for read or "10" for write. For read operation, the device address must match the address of the target PHY device. For write operation, the address may be all zero or match a specific PHY address. Turnaround cycle is an idle cycle consists of two bit times between the register address field and data field in order to
3.8.2 PHY address
MTD972 uses 5 bits as PHY address, so there are 32 possible PHY address. The address is latched into internal register during reset from the pin setting. If MTD972 latches an address "00000", it is put into isolation mode. For an MII operation with address field "00000", the operation is treated as broadcast.

4.0 REGISTER DESCRIPTIONS

4.1 Control Register (CR 00H)

00.15  RST  Reset
Setting this bit causes a software reset operation in the PCS portion of the logic.
RW/SC  0

00.14  LBK100  Loop Back Enable for the 100TX PHY
Loopback the transmit data to the receive data. MTD972 exercises the loopback at the most extensive way. The serialized transmit bit stream at 125MHz is looped back to the received CRM.
Setting this bit high also asserts the internal signal_status and restart the synchronization process of the descrambler. MTD972 should be isolated from the media in this loopback mode.
RW  0

00.13  SPD  Speed Select
If ANE is 0, then this bit select the link speed.
If ANE is 1, this bit is ignored.
1=100Mb/s, 0=10Mb/s
RW  1

00.12  ANE  Auto-Negotiation Enable
Set to 1 to enable Auto-Negotiation operation
RW  1

00.11  PWD  Power-Down
Set to 1 for power down operation.
RW  0
* This has no effect in MTD972. No power down mode is implemented in MTD972.

00.10  ISO  Isolate
Setting this bit will isolate the MTD972 from the MII bus.
Specifically, all outputs RX_CLK, RX_DV, RX_ER, RXD, COL, CRS, TX_CLK are tri-state, and inputs TX_EN, TX_ER, TXD are ignored. The management port of MII is still active.
RW  0

00.09  ANR  Auto-Negotiation Restart
Setting this bit cause the auto-negotiation process to be restarted. It is cleared when auto-negotiation process is finished. This bit has no effect if ANE=0.
RW/SC 0

00.8 FDX Full Duplex
Setting this bit high when ANE=0, select the full-duplex operation. If ANE=1, this bit reports the
duplex selection of auto-negotiation.
RW 1
* Note for ANE=1. This bit is the same as 01.14.

00.7 CLT Collision Test
Setting this bit cause the COL signal to be asserted when TX_EN is asserted.
RW, 0

4.2 Status Register (SR 01H)

01.15 T4C 100BaseT4 capability
RO, P 0

01.14 TXF 100BaseTX Full-Duplex capability
RO, P 1

01.13 TXH 100BaseTX Half-Duplex capability
RO, P 1

01.12 TFC 10BaseT Full-Duplex capability
RO, P 1

01.11 THC 10BaseT Half-Duplex capability
RO, P 1

01.6 MFP MF Preamble Suppression
MTD972 does not support the management interface without preamble pattern.
RO, P 0

01.5 ANC Auto-Negotiation Complete
This bit reflects the status of auto-negotiation process.
RO, SC 0
* This bit is read 0 if ANE=0.

01.4 RFS Remote Fault status
This bit is set to indicate a remote fault condition has been detected. This bit should be cleared
every time this register is accessed. It is also set if the link word received from the link partner
with RF bit set (05.13).
RO, L 0

01.3 ANA Auto-Negotiation Ability
MTD972 has this ability
RO, P 1

01.2 LNK Link Status
This bit is set that if a valid link is established either as 100TX or 10BaseT. The bit has a
latching function that once it is reset to indicated link fail, it remains cleared until the register is
accessed.
RO, L 0
01.1 JAB
This bit is set that if a jabber condition is detected in 10BaseT operation. This has the same
latching feature as LNK bit.
RO, L 0

01.0 EXT Extended Capability
MTD972 support the extended register function
RO, P 1

4.3 PHY Identifier Register 1 (PIR1 02H)
This register contains the OUI information.

4.4 PHY Identifier Register 2 (PIR1 03H)
This register contains the OUI information.

4.5 Auto-Negotiation Advertisement Register (ANAR 04H)

04.15 NP Next Page Indication
This bit should be set when the register contains the next page information. This bit should be
set if local MTD972 want to engage the next-page exchange with its link partner. This bit also
represent the NP filed of transmitted base link code word.
RW, 0

04.14 ACK Acknowledge
This bit is controlled by MTD972 during the auto-negotiation process. Writing to this bit has no
effect. Reading this bit reflect the ACK bit status of auto-negotiation.
RO, 0

04.13 RF Remote Fault
This bit is set by management to indicate that a remote fault condition is detected.
RW, 0

04.9 T4 100BaseT4 capability
MTD972 does not support 100BaseT4.
RO, P 0

04.8 TXF 100BaseTx Full-duplex capability
This bit is set by the management.
RW, 1

04.7 TXH 100BaseTx Half-duplex capability
This bit is set by the management.
RW, 1

04.6 TBF 10BaseT Full-duplex capability
This bit is set by the management.
RW, 1

04.5 TBH 10BaseT half-duplex capability
This bit is set by the management.
RW, 1
04.4:0 SLF Selector Filed
This five bit should be set to identify the type of message
sent by auto-negotiation.
00001: IEEE 802.3
00010: IEEE 802.9
All other combination are reserved.
RW, 00001

4.6 Auto-Negotiation Link Partner Ability Register (ANLPAR 05H)

05.15 NP Next Page Indicate
This bit is set when the partner wish to engage in next page transfer.
RO, 0

05.14 ACK Acknowledge
This bit is the ACK bit received from the link partner. It is set by the link partner when it
acknowledge the reception of the link code word.
RO, 0

05.13 RF Remote Fault
This bit is the RF bit received from the link partner. It is set by the link partner when it detect a
remote fault condition. This bit also control the RFS bit in basic status register.
RO, 0

05.9 T4 100BaseT4 capability
This bit is set by link partner when it support 100BaseT4.
RO, 0

05.8 TXF 100BaseTx Full-duplex capability
This bit is set by link partner when it support 100BaseTX full duplex.
RO, 0

05.7 TXH 100BaseTx Half-duplex capability
This bit is set by link partner when it support 100BaseTX half duplex.
RO, 1

05.6 TBF 10BaseT Full-duplex capability
This bit is set by link partner when it support 10BaseT full duplex.
RO, 0

05.5 TBH 10BaseT half-duplex capability
This bit is set by link partner when it support 10BaseT half duplex.
RO, 0

05.4:0 SLF Selector Filed
This is the bit received from the link partner indicating the protocol selection.
00001: IEEE 802.3
00010: IEEE 802.9
All other combination is reserved.
RO, 00000

*This register is also used to receive the next page information. In this case the meaning of this register is
redefined as following
05.15  NP    Next Page Indicate
This bit is set when the partner has additional next page to transmit.

05.14  ACK   Acknowledge
This bit is the ACK bit received.

05.13  MPG   Message Page
This bit is set if a coded message.

05.12  ACK2  Acknowledge 2
This bit is set by the link partner if it will comply with the received message.

05.11  TGL   Toggle
This bit is used to maintain synchronization of the next page transfer.

05.10:0  DAT  Data
Data can either be a coded message or unformatted page.

4.7 Auto-Negotiation Expansion Register (ANER 06H)

06.4  PDF   Parallel Detection Fault
This bit is set by the auto-negotiation process if a parallel detection fault has occurred. That is
none or more than one of the NLP, 100BaseTX have indicated link ready. This bit has a
latching function and is cleared by accessing this register.
RO, L0

06.3  LPNPA Link Partner Next Page Ability
This bit is set when received base link code work from the link partner has its NP bit set.
RO, 0

06.2  NPA   Next Page Ability
MTD972 support the next page function. This bit is used to control the autonegotiation arbiter
state machine.
RO, P 1

06.1  RCV   Page Received
This bit is set to indicate that a new link code word is received and stored in ANLPAR. This bit
is cleared when ANLPAR is read.
RO, L0

06.0  LPANA Link Partner Auto-Negotiation Ability
This bit is set if MTD972 detect that its link partner support auto negotiation.
RO, 0

4.8 Auto-Negotiation Next Page Transmit Register (ANNPTR 07H)

07.15  NP    Next Page
This bit is set to indicate that additional pages is to be transmitted.
RW, 0

07.14  ACK   Acknowledge
This bit is controlled by the auto-negotiation process of MTD972.
RO, 0
07.13 MPG  Message Page
This bit is set to indicate the data contained is a coded message.
RW, 1

07.12 ACK2  Acknowledge 2
This bit is set to indicate that local device is able to comply the coded message just received.
RW, 0

07.11 TGL  Toggle
This bit is controlled by the auto-negotiation process of MTD972.
RO, 0

07.10:0 DAT  Data
This is a 11 bit data field contains either coded message or unformatted information.

4.9 Disconnect Counter Register (DCR 12H)
This register contains the partition count

4.10 False Carrier Sense Counter Register (FCSCR 13H)
This counter is incremented when a false carrier sense condition is detected. A false carrier sense condition is meant that a frame is not started with /J/K/ symbol.
RO, SC 0000H

4.11 Receive Error Counter Register (RECR 15H)
This counter is incremented when a receive error condition is detected. A receive error include the DATA ERROR, PREMATURE END during valid packet reception.
RO, SC 0000H

4.12 Revision Register (RR 16H)
This register contains the revision number of MTD972.
RO, P 0000H

4.13 PHY Configuration Register (PCR 17H)

17.15 NRZIEN  NRZI Encoding/Decoding
This bit controls the NRZI encoding and decoding function.
If cleared, the NRZI encoding and decoding function is bypassed.
RW, 1

17.14 TOSEL  Descrambler Time Out Select
This bit is set to 1 to select Time out time as 2000us.
If it is 0, then the time out is 722us.
RW, 0

17.13 TDIS  Descrambler Time Out Disable
This bit is set to disable the time out counter in the descrambler.
RW, 0

17.12 RPTR  Repeater
This bit should be set for repeater application. In this case, CRS output only reflect the receive activity.
RW, CRSSEL
17.11 ENCSEL PMD ENCSEL control
This bit is used to control the output on ENCSEL pin.
RW, 0

17.8 20MENB  20MHZ output enable
This bit is set to enable the 20MHz output. Default is disable.
RW, 0

17.7 25MDIS  25MHZ output disable
This bit is set to tristate the 25MHz output. Default is enable.
RW, 0

17.6 FGLNKTX  Force good link in 100BaseTx mode
If this bit is cleared, the 100BaseTx PMA link status is forced to be in ready state.
RW, 1

17.5 FCONNT  Bypass the Disconnect function
This bit is set to bypass the disconnect function.
RW, 0

17.4 TXOFF  Transmit Off
This bit is set to turn off the 100BaseTx output in an idle state.
RW, 0

17.2 LEDTSL  LEDT display function select
If this bit is set to 1, then LEDT indicates the status of disconnect function.
RW, 0

17.1 LEDPSL  LEDP display function select
If this bit is set to 1, then LEDP indicates the full duplex operation of 10BaseT.
If this bit is set to 0, then LEDP indicates the polarity of 10Mb/s, or the FDX in 100Mb/s.

4.14 Loopback and Bypass Control Register (LBCR 18H)

18.14 BP4B5B

18.13 BPSCRM

18.12 BPALGN  Bypass Symbol Alignment

18.11 LBK10  Loopback control for 10BaseT
This bit is set to perform loopback test in 10BaseT section.
RW, 0

18.9 LBK1  Loopback control 1 for PMD
RW, 0

18.8 LBK0  Loopback control 0 for PMD
RW, 0
### LBK1 LBK0 Mode

<table>
<thead>
<tr>
<th>LBK1</th>
<th>LBK0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>PMD loopback, pin LBK is asserted</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Remote loopback.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

18.6 **FDCRS**  
Full Duplex CRS function
This bit is set to allow CRS to be asserted only to transmit activity in full-duplex mode operation.
For normal mode, this bit is set to 0 and only receive activity will assert the CRS in full-duplex.  
RW, 0

18.4 **CERR**  
Code Error
This bit is used to control either RXD[3:0] = 5H or 6H, when RX_ER is asserted.  
RW, 0

18.3 **PERR**  
Premature Error
This bit is used to control either RXD[3:0] = 4H or 6H, when RX_ER is asserted.  
RW, 0

18.2 **LERR**  
Link Error
This bit is used to control either RXD[3:0] = 3H or 6H, when RX_ER is asserted.  
RW, 0

18.1 **FERR**  
Frame Error
This bit is used to control either RXD[3:0] = 2H or 6H, when RX_ER is asserted.  
RW, 0

* Frame error is referred as 722 uS timeout in describer.

### 4.15 PHY Address Register (PAR 19H)

19.10 **ANS**  
State of Auto-Negotiation
R, O

19.8 **FEFE**  
Far End Fault Enable
This bit is set for enabling Far-End Fault function.
RW, 0

19.7 **DPLX**  
Duplex status
This bit reflect the duplex status of the link.
RO, 0

19.6 **SPD**  
Speed status
This bit reflect the speed selection of the link.  It is 1 for 10BaseT and 0 for 100BaseTx.
RO, 0

19.5 **CONN**  
Connection Status
This bit reflect the status of the disconnect function.

19.4:0 **PHYAD**  
PHY address
These four bits are the PHY address.
RO, PHYAD

---

MTD972 Revision 0.7 06/17/1997
4.16 10Base-T Status Register (10SR 1BH)

1B.9 10BTSER Serial mode for 10BaseT interface
This bit controls the serial mode operation of 10BaseT
RW, 10BTSER

1B.0 POLST Polarity state
RO, 0

4.17 10Base-T Control Register (10CR 1CH)

1C.5 LOE Link Pulse Output Enable
This bit controls the output of link pulse in 10BaseT mode. This bit does not affect the output of
FLP in Auto-Neg.
RW, 1

1C.4 HBE Heartbeat Enable
This bit controls the Heartbeat function of 10BaseT PMD.
RW, 1

1C.3 UTPV This bit controls the either TPOV or TPOI output. Set to
1 for TPOV, and 0 for TPOI
RW, 1

1C.2 LSS Low Squelch Select
This bit has no effect.
RW, 0

1C.1 PENB Polarity Enable Control
This bit when set 0 enables the polarity correction of the 10BaseT transceiver.
RW, 0

1C.0 JEN Jabber Enable
This bit controls the Jabber function in the 10BaseT PMD.
RW, 1

5.0 ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idd</td>
<td>-</td>
<td>150</td>
<td>220</td>
<td>mA</td>
</tr>
</tbody>
</table>

**MII Interface**

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vih, MII</td>
<td>2.0</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Vil, MII</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Voh, MII</td>
<td>2.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Vol, MII</td>
<td>-</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

**PMD Interface**

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vih, ECL</td>
<td>Vdd-1.16</td>
<td>-</td>
<td>Vdd-0.88</td>
<td>V</td>
</tr>
<tr>
<td>Vil, ECL</td>
<td>Vdd-1.81</td>
<td>-</td>
<td>Vdd-1.47</td>
<td>V</td>
</tr>
<tr>
<td>Voh, ECL</td>
<td>Vdd-1.00</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Vol, ECL</td>
<td>-</td>
<td>-</td>
<td>Vdd-1.62</td>
<td>V</td>
</tr>
<tr>
<td>Name</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td>Unit</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td><strong>10BaseT Transceiver</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vts, UTP input squelch</td>
<td>+/- 200</td>
<td>+/- 250</td>
<td>+/- 300</td>
<td>mV</td>
</tr>
<tr>
<td>Vto, UTP output voltage</td>
<td>+/- 2.2</td>
<td>+/- 2.5</td>
<td>+/- 2.8</td>
<td>V</td>
</tr>
<tr>
<td>(Voltage mode TPOVP/TPOVN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ito, UTP output current</td>
<td>+/- 88</td>
<td>+/- 100</td>
<td>+/- 112</td>
<td>mA</td>
</tr>
<tr>
<td>(current mode TPOIP/TPOIN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 5.2 AC Characteristics

#### Reset Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Reset Time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>us</td>
</tr>
</tbody>
</table>

#### Clock Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFIN to TX_CLK delay</td>
<td>2.0</td>
<td>4.5</td>
<td>6</td>
<td>nsec</td>
</tr>
<tr>
<td>TX_CLK duty cycle</td>
<td>45</td>
<td>-</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>RX_CLK duty cycle</td>
<td>45</td>
<td>-</td>
<td>55</td>
<td>%</td>
</tr>
</tbody>
</table>

#### MII Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_EN, TX_ER, TX_D to TX_CLK rise setup time</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>nsec</td>
</tr>
<tr>
<td>TX_EN, TX_ER, TX_D to TX_CLK rise hold time</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>nsec</td>
</tr>
<tr>
<td>RX_CLK rise to RX_DV, RX_ER, RX_D delay</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>nsec</td>
</tr>
</tbody>
</table>

#### 100Mbs Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total transmit and receive latency</td>
<td>-</td>
<td>-</td>
<td>170</td>
<td>nsec</td>
</tr>
</tbody>
</table>

#### 10Mbps Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heartbeat delay</td>
<td>0.8</td>
<td>-</td>
<td>1.2</td>
<td>usec</td>
</tr>
<tr>
<td>Heartbeat duration</td>
<td>0.8</td>
<td>-</td>
<td>1.2</td>
<td>usec</td>
</tr>
<tr>
<td>Jabber turn-on time</td>
<td>20</td>
<td>-</td>
<td>40</td>
<td>msec</td>
</tr>
<tr>
<td>Jabber reset time</td>
<td>500</td>
<td>-</td>
<td>650</td>
<td>msec</td>
</tr>
<tr>
<td>Link pulse width</td>
<td>80</td>
<td>100</td>
<td>150</td>
<td>nsec</td>
</tr>
<tr>
<td>Link pulse duration</td>
<td>8</td>
<td>16</td>
<td>24</td>
<td>msec</td>
</tr>
</tbody>
</table>

#### Auto-Negotiation Timing

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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<tbody>
<tr>
<td>FLP clock period</td>
<td>100</td>
<td>125</td>
<td>150</td>
<td>usec</td>
</tr>
<tr>
<td>FLP clock data delay</td>
<td>60</td>
<td>63</td>
<td>70</td>
<td>usec</td>
</tr>
<tr>
<td>FLP clock/data pulse width</td>
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<td>75</td>
<td>-</td>
<td>nsec</td>
</tr>
<tr>
<td>FLP burst period</td>
<td>-</td>
<td>16</td>
<td>-</td>
<td>msec</td>
</tr>
<tr>
<td>FLP burst width</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>msec</td>
</tr>
</tbody>
</table>
6.0 PACKAGE DIMENSION

100 PIN QFP  Unit: inch

[Diagram of 100-pin QFP package dimensions]