A Universal Controller for Distributed Control of Power Electronics Systems in Electric Ships

Gerald W. Francis, *Student Member, IEEE*, Rolando P. Burgos, *Member, IEEE,* Ivan Celanovic, *Member, IEEE,* Fred Wang, *Member*, *IEEE*, and Dushan Boroyevich, *Member, IEEE*.

***Abstract*—This paper presents a distributed control system architecture for power electronics conversion systems. Control partitioning is explored under this scheme by analyzing spatial, temporal, and functional aspects of a family of power converters, finally proposing a two level control hierarchy. Specifically, a hardware manager –controlling the actual power conversion process–, and an application manager, hardware independent Universal Controller are introduced and implemented. A detailed description of these controllers is given using a voltage-source inverter as test system. Additionally, a high-speed real-time protocol (PESNet) is introduced for communication purposes of the proposed distributed control architecture. From the analysis presented the usage of such an architecture and controllers for reconfigurable zonal distribution systems becomes apparent.**

I. INTRODUCTION

In recent years, power electronics has been steadily moving towards developing an integrated systems approach in the design and manufacturing of power electronics components and subsystems [1-3]. One of the first coordinated research and development efforts in that direction has been the Power Electronics Building Block (PEBB) program, envisioned by the Office of Naval research (ONR) [3].

The main idea behind the PEBB concept is to design a minimal set of multifunctional, flexible and easy-to-use power electronics modules capable of operating in a wide range of applications [3]. To achieve this enhanced flexibility- though PEBB modules need enough integrated intelligence to enable a simple, straight forward reconfiguration of their functions [3-4]. These capabilities combined with the standardization of their electrical and mechanical interfaces brings unparalleled modularity to power electronics systems, allowing for simple system reconfiguration and a "Plug and Play" (PnP) system design approach [5]. All highly desirable features for modern more electric ship power systems.

Interestingly enough, while there has been a significant effort to integrate and modularize switching power converters, the control architecture of power electronics systems has not evolve correspondingly. In fact, both control hardware and software are most often custom designed with very little modularity and flexibility. Regarding the controller itself, the vast majority of today's digital controllers present system architectures heavily dependent on converter topology, power level, and type of application [6]. This brings us to the conclusion that control architecture is one of the main roadblocks toward envisioned flexible and multifunctional building block based power electronics.

In this work, we aspire to lay a general foundation for the control of PEBB-based power electronics systems using an open-system distributed control architecture. Instead of using a centralized approach, we propose to split and distribute control authority between power modules, the application controller (higher level controller), and the communication network. Furthermore, we propose new standardized interfaces between these control modules, which bring openness together with the desired reconfiguration capability to the whole system.

The concept of distributed control has been widely accepted by the motion control industry and factory automation systems [7]. However, distributed control at the power converter level has not yet been studied in a great detail. In [8], a distributed digital controller for high-power drives was proposed. The controller was partitioned into a regulator and a bridge controller connected via a relatively slow parallel bus. A different approach was proposed in [9], where the control structure was split between a modular controller (converter phase-leg) and an outer loop controller connected this time using a 2.5 Mb/sec daisy-chained fiber optic link. In this paper a dual fiber optic ring

This work was supported by the Office of Naval Research under Grants N00014-00-1-0489 and N00014-03-1-0771. This work made use of ERC shared facilities under award number EEC-9731677.

G. W. Francis is with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA e-mail: jerryf@vt.edu).

Rolando Burgos is with the Center for Power Electronics Systems, Virginia Polytechnic institute and State University, Blacksburg, VA 24061 USA (email: rp.burgos@ieee.org)

Ivan Celanovic is with the Massachusetts Institute of Technology, Cambridge, MA, 02139 (email ivanc@mit.edu)

Fred Wang is with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (email wangfred@vt.edu).

Dushan Boroyevich is with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (email dushan@vt.edu).

network connects the power modules (converter phase-legs) with the application controller, thus providing enhanced reliability to the control system.

This paper is organized as follows. In section II we introduce the notion of power electronics system distribution and explain the motivation for control authority partitioning as well as basic analysis of the system distribution. Section III presents control architecture design issues of the architecture employed, using the design of a three-phase voltage source inverter (VSI) as an example. Section III also presents a prototype system built using a distributed controller approach and some of its performance limitations. The final section summarizes the findings of the paper.

II. Control Architecture Partitioning

A power electronics system can be characterized for distribution purposes in three dimensions, namely functional, temporal and spatial [12]. Such a system classification has been extensively explored in computer science and systems [10], which similarly to power electronics also exhibit three dimensions, namely hardware, control and data.

The functional distribution of power converters depends on the respective power stage topology, application requirements, and control algorithms. Power converters also exhibit a strong and easily identifiable temporal distribution, which is basically defined by protection devices, electro-mechanical time constants, sampling frequency and several controls bandwidths. Spatial distribution on the other hand is strongly dependant from the converter power level and specific system requirements. Fig. 1 shows a block diagram of a typical power electronics system illustrating both temporal and functional distributions. The spatial distribution, not shown in this picture, is very pronounced for medium and high power applications, playing a significant role in the design of controls architecture.

Any power electronics system intrinsically presents all three types of distributions. In this paper however we have only focused on studying the control system of power converters, having as main goal the development of a distributed control system architecture. The proposed control architecture can be applied to numerous types of converters, however some or all its benefits may be impossible to attain if the system itself is incorrectly partitioned.

In this paper we propose a distributed controller architecture which partitions control authority between the hardware manager (HM), the application manager (AM)

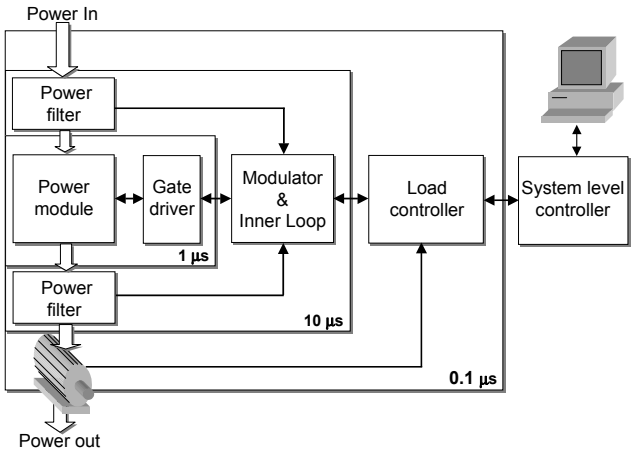

Fig. 1. Block diagram of typical power converter control architecture.

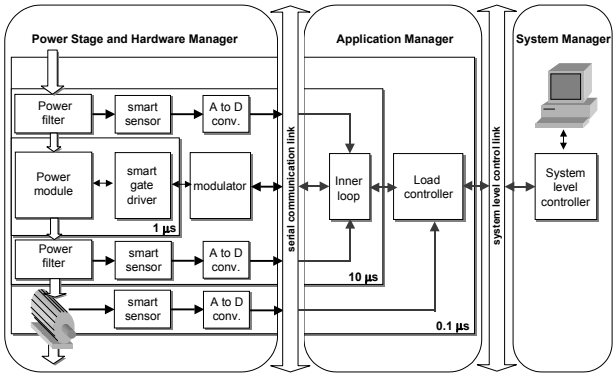

Fig. 2. Proposed distributed control architecture dividing control authority between hardware, application and system managers.

and system manager (SM) as shown in Fig. 2. The hardware manager is designed to handle fast and hardware oriented control tasks. The HM becomes an integral part of the power processing hardware thus making it "intelligent" and transparent to the user. The AM on the other side is designed to assume higher level control tasks, such as inner loop and load control, and is designed to be converter independent. The SM performs system level control and monitoring and doesn't have to be always implemented.

A. Topology Partitioning and HM integration

Although there is a large number of different topologies and physical realizations in the set of applications under consideration (some of which are depicted in Fig. 3.), certain common denominators do exist among them. These can be identified as follows. Semiconductor power devices in general behave as single-pole single-throw (SPST) switches. Yet, from a functional point of view, the converter can be represented using single-pole multiple-throw (SPMT) switches. This is possible due to complementary

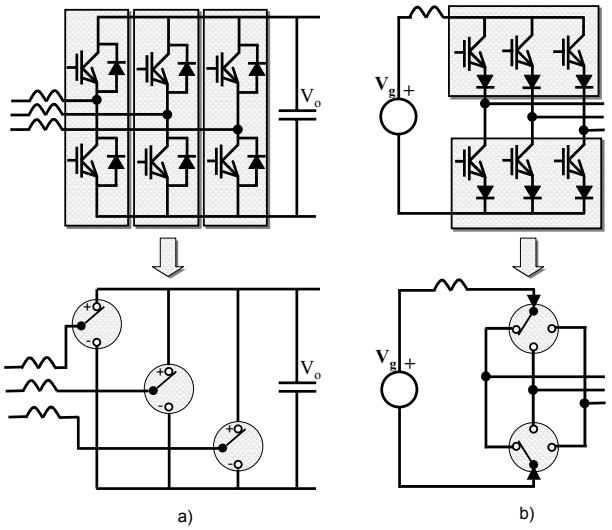

Fig. 3. Functional switch assemblies on the with three-phase converter examples: a) boost rectifier, b) current source inverter.

relationship that exists between the switches on each phase. For example, although the three-phase converter shown in Fig. 3 has six SPST switches, considering its topological constraints it may be represented by only three SPDT switches. The three-phase buck converter on the other hand may be represented with two SPTT switches. Then, since we have an isolated SPDT switch as basic building block in most voltage-source topologies, we can use the same token and have the HM be the basic control function associated to it, a converter phase-leg.

The main task of the HM is hence to control the power switches of its corresponding phase-leg mimicking the operation of an SPDT switch. Although the physical realization of an ideal SPDT switch or any super set of SPDT switches can vary significantly, the HM should make this hardware specific implementation issues transparent to the AM. This approach to control authority partitioning directly decouples controller tasks and lends itself to an open, modular, PnP design approach.

III. Control Architecture Design

An example of the previous discussion is shown in Fig. 4, in the form of a distributed control architecture for a three-phase PWM-VSI. The following sections describe in detail its implementation.

A. Communications Protocol

The communication protocol between the application manager and hardware managers is designed as a master-slave ring network that runs at 125 Mb/s over plastic optical fiber [14-15]. Under this type of network structure, the application manager is the master, and as such regulates all communications with the hardware managers, the slaves.

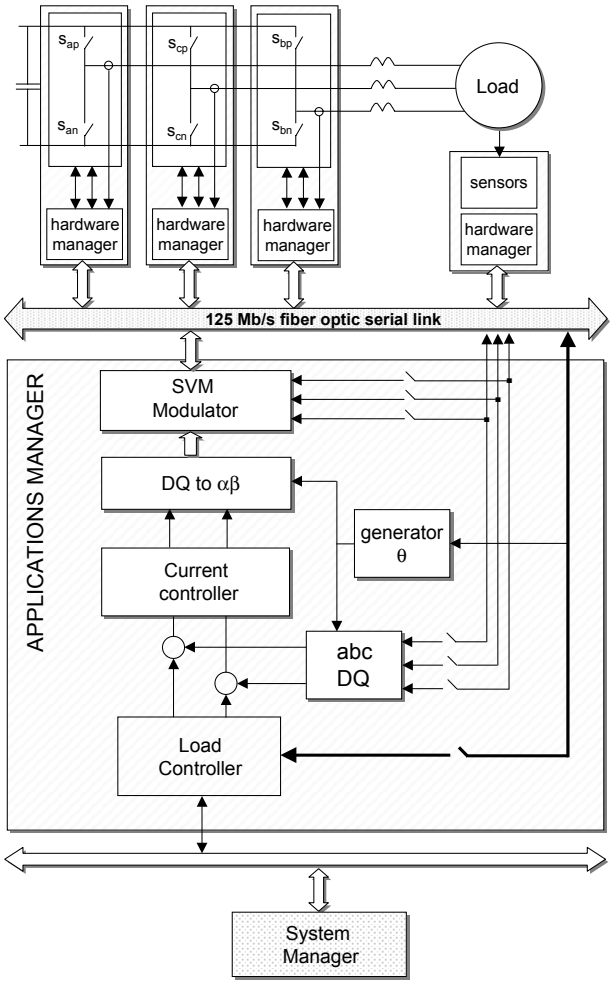

Fig. 4 Block diagram of distributed controller applied to a VSI.

A specific network protocol was designed and proposed for this purpose in [14], PESNet, having the following features: a deterministic network response, a large communication throughput, a precise node synchronization, and an open network architecture. All the control variables, namely switching frequency, duty cycles, and different sensor readouts are transmitted on every switching cycle. Provision for non-critical data transfer additionally supports tasks such as initialization and software reconfiguration of the hardware managers.

In the first version of PESNet, there were three types of time critical data frames, the control data, synchronization, and command frames. The data frame consists of a command indicating the beginning of the data packet, the address of the slave node, the actual data field, and an error check. The way the data field is configured depends on the particular application and type of hardware manager. A more detailed explanation of the communication protocol can be found in [12][14-15]. A second revision of this protocol has been designed and implemented, adding a fault tolerance capability to it [21].

B. Hardware Manager

This section describes the design and implementation of two types of hardware managers, a switching module HM and a sensor HM. The switching module HM implements a soft-switched phase-leg for voltage-source converters. However, regardless of the specific switching cell implementation (number of switching modules, type of soft-switching, dead-time requirements etc.) this switch arrangement should ideally behave as a SPDT switch. Therefore the control information received from the AM is independent of the actual implementation. The sensor HM is designed for voltage and current sensor and makes data acquisition transparent for the AM. More details can be found in [11-12].

The hardware manager is designed to control soft-switched phase leg that consists of two IGBT phase-leg (main and auxiliary) modules and an LC resonant tank. This type of hardware manager has the following functions:

- PWM generation for main and auxiliary switches
- Isolated gate drivers for main and auxiliary switches
- Over-current, voltage and temperature protection
- Current, voltage and temperature sensing
- Communication of PWM, status and measurement information via an optical communication link.

The only interface that the hardware manager needs to communicate is a standardized serial data packet explained in previous section. All the necessary data for proper module operation are encoded in the data field of the control data packet.

The first revision of the hardware manager consists of gate drives, a high speed ALTERA 10K EPLD, two A/D converters, a high-speed ECL logic data transmitter and receiver, and a 125 Mb/sec optical transceiver. The communication interface within the hardware manager is built in three layers (according to ISO/OSI reduced reference model) defined as: physical layer, data link layer and application layer. The physical layer is provided by means of an inexpensive plastic optic fiber, while the interface between the data link layer and the physical layers are achieved using Hewlett Packard optical transceivers. The data link layer is provided by the TAXIchipTM' (transmitter and receiver) [16]. An incoming optical signal is fed to the transceiver and then to the TAXIchipTM [16] receiver. The receiver converts the serial stream into parallel, which is then loaded into the PLD for final data processing. Similarly, outgoing data from the PLD (in parallel form) are converted by the TAXIchipTM transmitter into a serial stream, amplified by the optical transceiver [17] and transmitted through the optical fiber.

A PWM generator and local fault protection are also realized in the PLD onboard the HM. Three main parameters necessary for proper operation of PWM generator are: duty cycle, switching period and the synchronization command. The duty cycle data, when received and validated for proper transmission, is stored in an input register. The duty cycle becomes active only after it receives a synchronization command from the AM, which relocates the duty cycle information to the executable buffer used for PWM generation.

Measurement of the module state variables (voltage and current) is performed simultaneously across all modules per switching cycle using two 12-bits AD converters, while the temperature measurement is performed at a slower rate. All the sampling times in the network are synchronized with respect to a network synchronization command issued via PESNet. Measurement results are stored an output buffer, ready to be packed into a corresponding data packet and sent back to the AM.

IV. Universal Controller

A universal controller (UC) has been designed that allows system designers to quickly create an implementation of control algorithms via the set of interfaces previously described by providing an adaptable platform for control software development [21]. The controller has several interfaces that facilitate control design and system compatibility.

A. DSP and CPU functions

The controller has a digital signal processor that can be used to implement control algorithms written in either assembly or C-code. The DSP is central to the converter control functions. To assist the DSP is an FPGA, which can be programmed to include control and timing functions that would be easier to implement in digital logic as opposed to C-code. The DSP should be relatively fast, as the converter control bandwidth can be several tens of Kilohertz.

B. System Level Interfaces

The controller must communicate with a higher hierarchy system controller in most applications. For instance to coordinate the operation of several motor drives, and setting application specific parameters. The UC has two main application level interfaces. The first one is a PMC (PCI mezzanine card) interface, in the form of a doublewide PCI mezzanine card (IEEE p.1386). The UC can therefore plug into a host carrier card, and be placed in a PCI or VME system. The second interface is a field bus interface connector. This connector can be used by placing the field bus interface on a daughter card and connecting it to the UC. The controller will then become a node on a field bus network such as Profibus or DeviceNet. In case these interfaces are not available, a synchronous serial interface is also available that directly connects to the DSP.

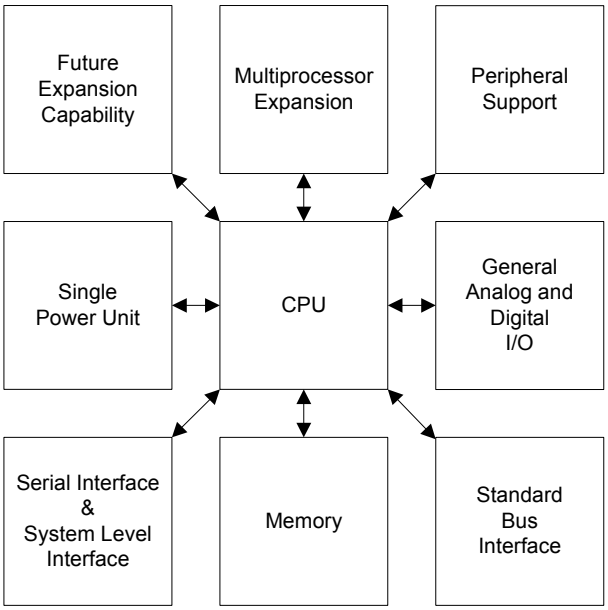

Fig. 5. Conceptual block diagram.

C. *Functional Expansion*

It is desirable that the UC has a way to expand its capabilities in case a specific function is required but not implemented. To address this, there are several ways in which the controller can expand. Firstly, if more processing power is needed, the UC is stackable with up to three other UC's to add processing capacity and board resources. The resources of the stacked controllers are accessible from any board to any other board totally transparently. Secondly, if a hardware function is not present, it is possible to interface it via an 88 pin bidirectional expansion connector. Since the UC does not have analog to digital converters, it may be desirable for a centralized control application to design a daughter board to attach to this expansion port.

D. *Storage and Memory*

In many applications, it is desirable to store data in nonvolatile memory, such as control parameters transmitted from a supervisory control system, system configuration information, and DSP code. The controller provides two Flash RAM components to implement this.

E. *UC Architecture*

The structure of the universal controller (conceptual block diagram based on requirements) is shown in Fig 5. The controller uses an Analog Devices ADSP-21160 DSP with a Xilinx XCV400 FPGA to perform high speed control tasks. Two fiber optic ring interfaces are made available via two Cypress CY7C9689 TAXI transceivers. The CY7C9689 combines the functionality of the previous AMD TAXI chips into one TQFP package. To ease debugging, two hexadecimal displays and a dual-channel DAC is provided. Eighty eight general-purpose I/O

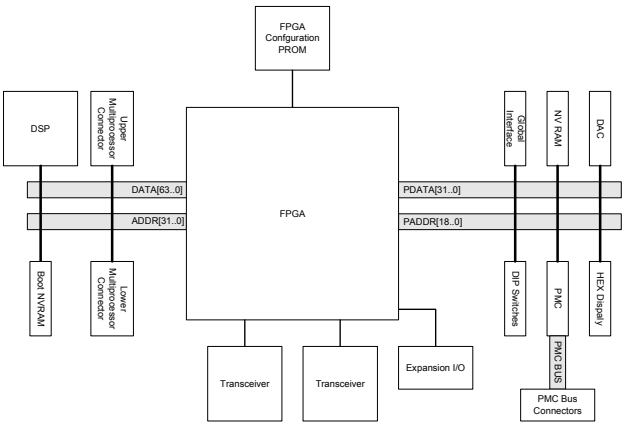

Fig. 6. Functional block diagram of Universal Controller.

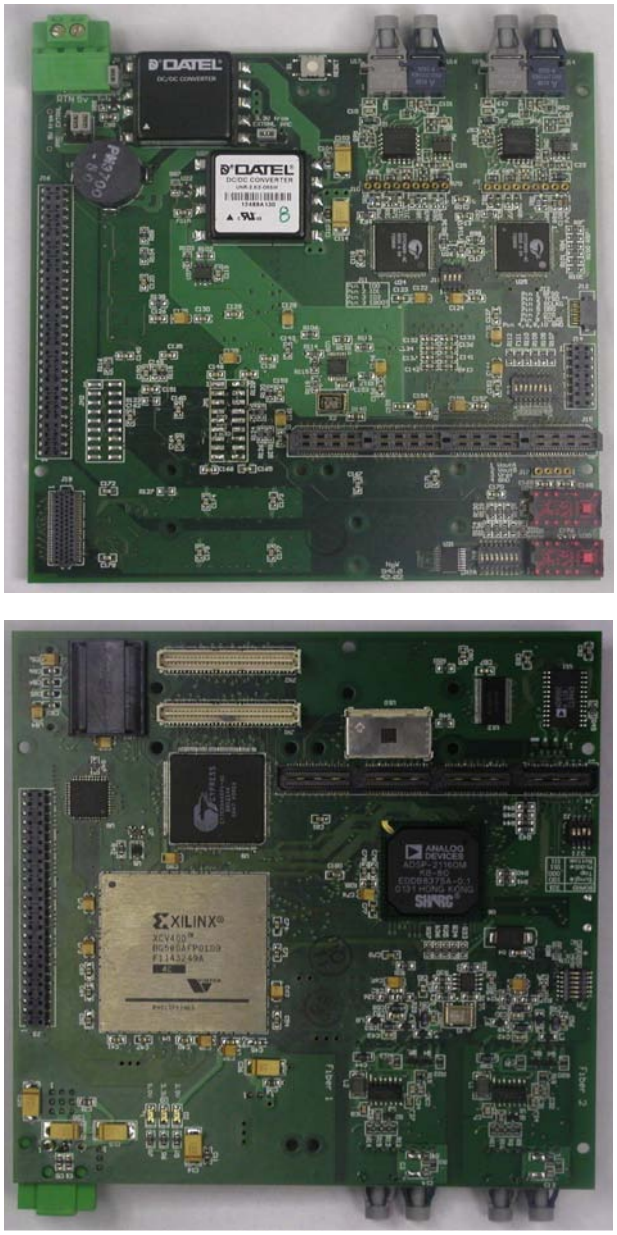

Fig. 7. Universal Controller.

pins make it possible to interface a large variety of applications, and is also very useful for debugging. Additional interfaces are available for programming, expanding, and interfacing the controller.

Functionally, the CPU is the central control unit on the UC. However, when it is implemented, an FPGA is used to coordinate all devices, as shown in Fig 6. After the controller was designed, two revisions of the controller were implemented and tested. The second revision of the controller is shown in Fig 7.

V. CONCLUSION

This paper has presented a distributed control system architecture and its implementation for power electronics conversions systems. The distributed architecture was built over two controllers, a hardware manager, and an application, hardware independent controller, dubbed Universal Controller. A detailed description of the latter was provided given its intrinsic suitability to implement different power conversion functions onboard electric ships. Its modularity and high processing capacity have made it a feasible alternative for such systems, where its ease of reconfiguration and independence from the actual type of application could be beneficially exploited.

REFERENCES

[1] J. D. Van Wyk and F.C. Lee, "Power Electronics Technology at the Dawn of the New Millennium-Status and Future," IEEE PESC Conference Proceedings, 1999, vol. 1, pp. 3-12,

[2] A. A. Jaecklin, "Future Devices and Modules for Power Electronic Applications," European Conference on Power Electronics and Applications, EPE, September 1999.

[3] T. Ericsen, A. Tucker, "Power Electronics Building Blocks and Potential Power Modulator Applications," IEEE Conference Record of the Twenty-Third International Power Modulator Symposium, New York, NY, 1998, pp. 12-15.

[4] T. Ericsen, "Open Plug and Play Power Architectures Simplifies System Integration," PCIM Magazine, pp. 70-71, February 2000.

[5] T. Ericsen, "Control Architectures and Distributed Intelligence for Plug and Play Power Blocks," PCIM Magazine, pp. 38-41, March 2000.

[6] V. Vlatkovic, and D. Borojevic, "Digital-Signal-Processor-Based Control of Three-Phase Space Vector Modulated Converters," IEEE Transactions on Industrial Electronics, June 1994, Vol. 41, No. 3, pp. 326-332.

[7] E. Bassi, F. Benzi, L. Lusetti, G.S. Buja, "Communication Protocols for Electrical Drives," IEEE IECON Proceedings, 1995, Vol. 2, pp.706-711.

[8] P.L.G. Malapelle, G. Torri, R. Moruzzi, A. Oliva, "A New, Modular, Programmable, High Speed Digital Control for Large Drives," IEEE IECON 20th International Conference on Industrial Electronics, Control and Instrumentation, 1994; vol.1, pp. p.210-14.

[9] J.A. Du Toit, A.D. Le Roux, J.H.R. Enslin, "An Integrated Controller Module for Distributed Control of Power Electronics," IEEE APEC'98 Proceedings, February 1998, pp. 874-880.

[10] Jeffrey J. P. Tsai, Yaodong Bi, Steve J. H. Yang and Ross A. W. Smith, "Distributed Real-Time Systems," New York: John Wiley & Sons, Inc.

[11] I. Celanovic, I. Milosavljevic, D. Boroyevich, G. Jinhong, R. Cooley, "A New Distributed Controller for the Next Generation Power Electronics Building Blocks," 15th Annual IEEE Applied Power Electronics Conference Proceedings, February 2000, pp. 889-894.

[12] I. Celanovic, "A Distributed Digital Control Architecture for Power Electronics Systems," M. S. thesis, Virginia Polytechnic Institute and State University, 2000.

[13] I. Milosavljevic, Z. Ye, D. Borojevic, C. Holton, "Analysis of Converter Operation with a Phase-Leg in Daisy–Chained or Ring Type Structure," IEEE PESC Conference Proceedings, June 1999.

[14] I. Milosavljevic, D., Borojevic., I. Celanovic, "Modularized Communication and Control Structure for Power Converters," 8th European Conference on Power Electronics and Applications, EPE, September 1999.

[15] I. Milosavljevic, "Power Electronics System Communications," M. S. thesis, Virginia Polytechnic Institute and State University, 1999.

[16] "TAXIchip™ Integrated Circuits," Data Sheet and Technical Manual, Publication#07370, AMD, April 1994.

[17] "Plastic Optical Fiber and HCS® Fiber Cable and Connectors for Versatile Link," Technical Data 5963-3711E, Hewlett Packard, November 1994.

[18] "FLEX 10K-Embedded Programmable Logic Family Data Sheet," San Jose, California: Altera Corporation, October 1998, ver. 3.13.

[19] Jeffrey J. P. Tsai, Yaodong Bi, Steve J. H. Yang and Ross A. W. Smith, "Distributed Real-Time Systems," New York: John Wiley & Sons, Inc.

[20] I. Celanovic, I. Milosavljevic, D. Boroyevich, G. Jinhong and R. Cooley, "A New Distributed Controller for the Next Generation Power Electronics Building Blocks," IEEE APEC Proceedings, February 2000, pp. 889-894.

[21] G. Francis, "A Synchronous Distributed Digital Control Architecture for High Power Converters," Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA 2004.