A New Distributed Digital Controller for the Next Generation of Power Electronics Building Blocks

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Abstract **The need for low-cost, high-reliability, modular, easy to use and maintain power electronics systems is fueling the drive for standardized power electronics building blocks (PEBBs). Increased power density, user-friendly design, multi-functionality and increased reliability are the major issues that are being investigated. This paper proposes a new distributed digital control architecture for medium and high power PEBBs. The proposed architecture features high level of flexibility, modularity and paves the way towards future Plug and Play power converter systems.**

I. INTRODUCTION

The need for low-cost, high-reliability, easy to use power processing devices is becoming more and more pronounced [1]. Long design cycles, complex maintenance, a lack of standardization and high cost are slowing down possibilities for wider proliferation of power converters.

Power electronics has reached the point where further advancement, in terms of wider application of converters can hardly be achieved unless the community is presented with easy to use, of the shelf, reliable and flexible power electronics modules [1], [2], [3]. These modules may not be optimal from the cost point of view, but they would solve the problem of long design cycles and low reliability. Having flexible and multifunctional power processing units that cover a wide range of applications would provide higher production volume, thus reducing manufacturing costs. Furthermore, that would enable power electronics solutions for a large number of specific applications that can not justify single application development costs.

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In order to fulfill these requirements, future power electronics converters should have several predominant features, such as:

- a high level of integration, to improve reliability and lower costs;
- flexibility, to provide the necessary level of system adaptability and multi-functionality;
- in-circuit programmability, to allow for simple software and hardware reconfiguration and use of one standardized module in different applications; and
- user-friendliness, to enable the wider engineering community to create their own applications, thus focusing engineering efforts towards system-oriented design.

What is needed to bring the whole concept to its full potential is a general solution for the controller that will be able to support all necessary functions. The widely used concept, relying on a centralized digital controller [5] has several major drawbacks [8], thus indicating the need for a different approach in controller design and implementation.

This paper therefore presents a new approach to the problem, utilizing the idea of a distributed controller, well-suited for medium and high-power converters and that is in full compliance with above-mentioned design guidelines.

The concept of a distributed controller has been explored in motion control systems [9], from which we initially borrowed the idea. The novelty of this approach is in the fact that we are designing a distributed controller on a power converter level, compared with a motion control network where motor and controller are treated as one smart actuator. This difference introduces new control and communication issues.

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Some work has already been done regarding the control and communication issues where a distributed controller has been implemented at the converter level. Malapelle et al. [7] proposed a distributed digital control for high-power drives, splitting the controller on a regulator (dedicated to motor control), and a bridge controller (providing necessary firing signals for bridge switches) connected with a relatively slow parallel bus. Toit et al. [6] have proposed a more advanced distributed control structure, where each phase leg is controlled by a separate controller. Vital data for operation of the system is being communicated between the controller and phase legs through the daisy-chained fiber optical link (2.5 Mbits/sec), while the current (and/or voltage) loop is being closed locally through the phase leg digital signal processor (DSP).

The distributed controller discussed in this paper proposes a new control partitioning that falls along the natural boundary of technical expertise. Control engineers focus on the application and system issues, not the actual power hardware control. While power electronic engineers focus on the power conversion hardware and not the application. The proposed architecture consists of an application manager and one or more hardware managers linked with a high speed (125Mbits/sec) fiber-optical daisy-chained network. The application manager, liberated from any hardware-oriented tasks becomes a universal and converter independent entity. While the hardware manager, designed as an integral part of the power stage, handles hardware-specific tasks and provides a high level of module adaptability.

II. CONCEPT OF DISTRIBUTED DIGITAL CONTROLLER

For an effective design that would have inherent reusability an object oriented hardware design strategy was adopted. Additionally, the technology that was to be exploited should lend itself to affordability. Consider a set of widely used power electronics converters given in Fig. 1. Partitioning them, on a phase-leg basis, a universal power converter building block cell can readily be identified. With this common switching cell, families of different switching power converters such as AC/DC, DC/AC, DC/DC and AC/AC can be constructed. Furthermore, modularization of the control structure consistent with this common building block identifies a need for an intelligent building block and an application level controller. The concept of a smart, universal, modular and flexible power conversion building block can be realized by integrating the common switching cell, the gate drivers, sensors and some local intelligence. . These two basic blocks (application controller and intelligent switching module) with a proper interface could cleanly be partitioned. This interface becomes the power of the design.

In general, universal interfaces can be designed with either parallel or serial bus. Parallel bus is expensive, bulky and EMI prone. By selecting a high-bandwidth serial communication interface, sensor feedback signals could be routed via digital communication simplifying interconnections and extending system flexibility. This also leverages emerging communication technology, which is expected to eventually lower cost.

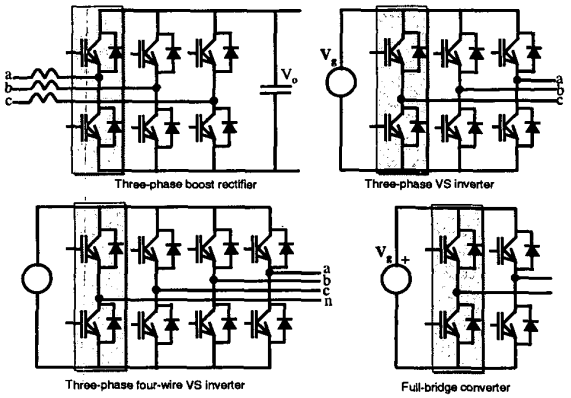

Fig. 1. Common converter topologies.

Within the integrated power module, the embedded control architecture together with gate drives, sensors, and communication interface is defined as the hardware manager. Consequently, the power building block consists of a common switching cell and its associated hardware manager.

By splitting the controller between power processing units and the main controller (Fig. 2.), defined as the application manager, a new component the communication link (interface I_1 in Fig. 2) is being introduced in to the control architecture. By means of open, flexible and high-bandwidth communication link the system will gain additional level of flexibility and adaptability.

Finally, a new distributed control architecture comprising three main components: application manager, hardware manager and communication link, shown in Fig. 2. can be established. One of the typical examples shown in Fig. 9, the three-phase Voltage Source Inverter (VSI), has been built and operated according to this control approach and will be discussed within this paper.

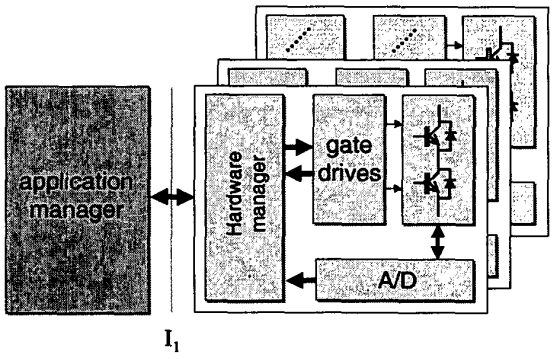

Fig. 2. New system architecture.

A. *Application Manager*

The application manager, envisioned as a high level controller liberated from any kind of low-level hardware oriented tasks, was designed to provide system flexibility and software re-configurability. It is specifically designed to perform higher-level control algorithms and supervisory tasks.

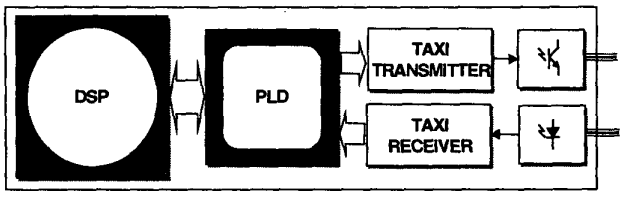

Fig. 3. Block diagram of new, universal controller.

As designed it consists of DSP processor, PLD and serial I/O port (shown in Fig. 3), which provides open control architecture capable of controlling multiple independent PEBB modules. The structure of the controller is totally independent of the converter topology, number of switches, sensors, etc. The DSP processor, which serves as a powerful yet flexible tool is designated for accomplishing application-specific tasks, thus yielding a high level of system adaptability.

System reconfiguration is achieved by simple software management. Providing an additional library of different programs for different control tasks would reduce development time and cost significantly, while reconfiguration of such a system then becomes solely a software-related issue.

B. *Hardware Manager*

The hardware manager, designed as an integral part of the PEBB module, is responsible for hardware related tasks such as: PWM generation, low level module protection, communication and sensing of all key analog variables. The hardware manager is application independent. Envisioned as an encapsulation of the hardware designers' knowledge to control and protect the power circuit. The vision is inclusive of the building block approach, meaning that the hardware manager itself should lend itself to hierarchical implementation.

Depending on the power level and system requirements the hardware manager can be designed for different power converter topologies or even sub-topologies. For example, the hardware manager can be designed for a single phase-leg or for a whole three-phase converter.

Once the communications interface is defined, this method of control partitioning allows the selection of the application controller based upon the application requirements and the hardware manager complexity based upon the topology and performance criteria. Both of which are programmable and reusable.

C. *Communication Link*

One of the gears that make the distributed controller system flexible, open, and modular is the communication protocol [8]. Our ultimate goal is to design a reliable, inexpensive, fast, and open control structure that would follow so-called "Plug and Play" (PnP) principles. The more information we communicate the more flexible a system we get, but since the bandwidth of the communication channel is limited, a trade-off has to be established. The communication network that we proposed and designed, together with the protocol, is based on the high-speed (125 Mbits/sec) daisy-chained serial fiber optic-link [8].

Two basic types of information are being communicated through network; real-time data, exchanged on switching cycle level, and initialization data exchanged during the system power up. Data that is being communicated from the application manager to the hardware manager is desired phase leg duty cycle and switching period. Feedback data is provided from the hardware manager to the application manager in the form of current, voltage, temperature and status information.

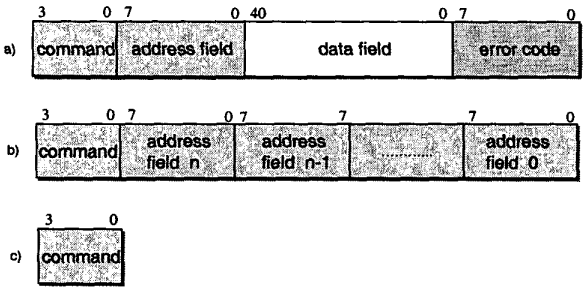

Fig. 4. Data formats in distributed controller network
a) data frame
b) synchronization frame
c) command frame

The format of the data packets that is being transmitted through the network is shown in Fig. 4. The specific number of bytes always follows a command that allows a receiver to identify the type of incoming data.

II. Implementation of Single Phase-Leg PEBB Based Hardware Manager

As previously explained, a single phase leg has been identified as the basic building block which provides good tradeoff between flexibility (defined as the number of realizable topologies with the basic cell) and added control and communication complexity.

For two-level converters, using the components described earlier as basic building blocks, topologies such as the full bridge converter, the three-phase VSI, or the three-phase boost rectifier can easily be assembled. For some multi-level topologies such as the flying capacitor, this cell can also be identified as a universal building block cell, while for others, such as neutral point clamped (NPC) converters, small changes are needed.

A. *Functional Description*

The hardware manager or "smart" gate drive is designed to perform several functions (Fig. 5) such as:

- PWM generation for main and auxiliary switches;
- Isolated gate-drive for both main and auxiliary switches;
- Over-current protection and indication;
- Current, voltage and temperature sensing and AD conversion; and
- Communication of PWM, status and measurement information.

The only information the power module communicates with is a standardized serial data packet going in and out of the module in a daisy-chain manner [8]. All the necessary data for proper module operation are encoded in the packet. Also, all the status information and sensed variables are sent back to the application manager, providing full control over converter operation.

If we impose a standard on the communicated data format, we can envision different manufacturer modules, connected into the same control network, controlled by single application manager, forming single or multiple converters that can drive one or more loads without conflict.

B. *Hardware Design*

The hardware manager, shown in Fig. 5, as designed consists of gate drives, a high speed ALTERA 10K PLD, two AD converters, a high-speed ECL logic data transmitter and receiver, and a 125 Mbits/sec optical transceiver on a single board. Its main role is to assure proper operation of the phase leg module in a daisy-chained control network and to provide all necessary information to the application manager for performing closed loop operation of all converters connected in a network.

The communication interface, within hardware manager is built in three layers (according to ISO/OSI standard) defined as: physical layer, data link layer and network layer

- Physical layer is provided by means of an inexpensive plastic optic fiber, while interface between data link layer and physical layer is achieved using HP optical transceiver.
- Data link layer is provided by TAXIchip™'s [10] (transmitter and receiver). An optical signal coming in signal, which is fed to the TAXIchip™ receiver. The receiver converts the serial stream into parallel, which then goes to the PLD the module is converted into a fast differential ECL.

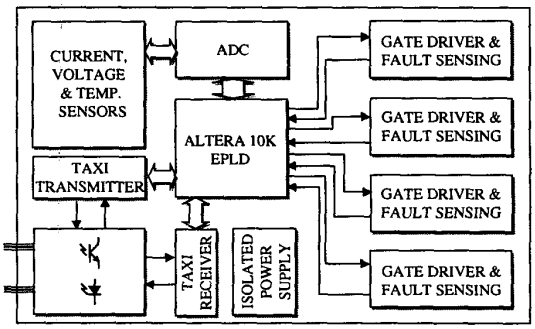

Fig. 5. Block diagram of designed hardware manager.

Similarly, outgoing data from the PLD (in parallel form) is transformed by the TAXIchip™ transmitter into a serial stream, and then amplified by the optical transceiver [11] and transmitted through the optical fiber.

- Communication and control block, which is implemented in hardware (PLD), handles all network layer functions. A block diagram of the implemented functionality is shown in Fig. 6. The communication and control subsystem can be viewed as a small RISC processor receiving commands through the network and executing commands. Its basic modes are described as:
  1. idle mode (waiting for the data packet),
  2. forward mode: when it is just passing the information to the following node,
  3. active mode (incoming data packet has the address of the node): when the data is being first verified by CRC checker and then stored in corresponding buffers and the packet is then forwarded with the results of current/voltage/temperature measurements and local status information,
  4. synchronization mode (after receiving SYNC command from application manager): which reloads the double buffers, initiates AD conversion and resets PWM generator and
  5. initialization mode: which initializes the whole system and dynamically assigns the node address.

PWM generator and local fault protection are also realized in the PLD. A functional block diagram is shown in Fig. 7. Three main parameters necessary for proper operation of PWM generator are: duty cycle, switching period and the synchronization command. The duty cycle, when received and validated for proper transmission, is being stored in

buffer 1. This information is becoming active only after a received synchronization command from the application manager, which moves the duty cycle information into buffer_2. Buffer_2 is active and is used for PWM generation. Period information (which controls switching frequency of the leg) is also double-buffered for the sake of proper synchronization. A digital comparator is comparing the content of the counter with duty cycle information and creating a control pulse for the switch. The dead time generator and fault protection are the final stages in PWM generation, providing shoot-through and over current/voltage/temperature protection.

Data acquisition subsystem is shown in Fig. 8. Most of today's control systems in power electronics are based on full-state feedback, which requires per-switching cycle current and voltage measurement. Therefore, the designed hardware manager consists of current, voltage and temperature sensors. Measurement of module voltage and current is performed simultaneously per switching cycle using two 12-bits AD converters, while temperature measurement is performed with 10 times slower rate. Proper timing is achieved through synchronization command received from application manager. Measurement results are stored in the output buffer, ready to be packed into a corresponding data packet. Onboard availability of these measurements allows for local current, voltage and temperature protection. All control functions and buffering are implemented within the PLD.

III. EXPERIMENTAL RESULTS

One of the biggest concerns when mixed-signal boards are designed for power control application is EMI noise immunity. Since the hardware manager is an integral part of the power module the circuit board will be mounted in close proximity to the IGBT modules (Fig. 10.), and will have to contend with high di/dt and dv/dt, due to the power device switching in excess of 20 kHz.

In order to verify the proper operation of the proposed system, the three-phase VSI was coupled with an RLC load. A block diagram of the VSI built from smart integrated phase-leg modules and controlled by the application manager through the high speed serial optical communication network is shown in Fig. 9. An actual converter photo is shown in Fig. 10. The three phase output voltage waveforms obtained from VSI operating in open loop are shown in Fig. 11.

IV. CONCLUSION AND FUTURE WORK

This paper presented a new approach for the control of medium and high-power converters. The new distributed controller architecture as proposed and implemented provides several prominent features:

- Hardware independent, universal controller capable of controlling multiple converters

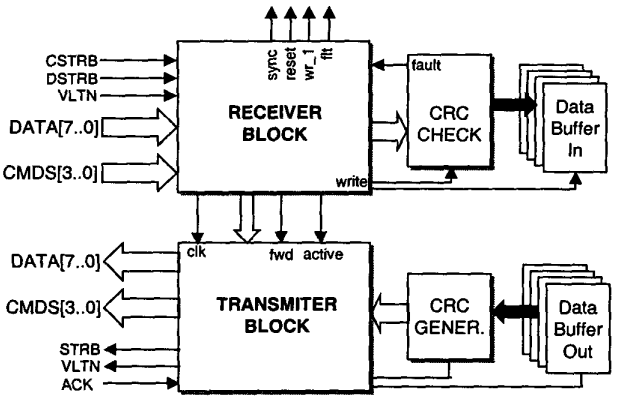

Fig. 6. Functional block of hardware manager controller implemented in PLD.

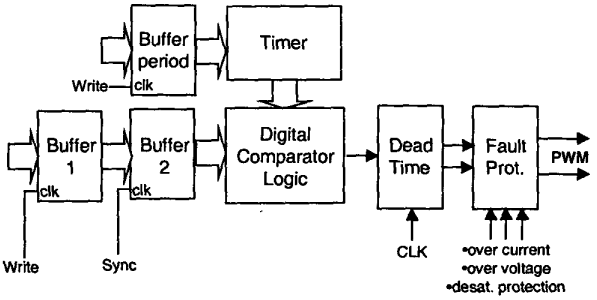

Fig. 7. Block diagram of PWM controller.

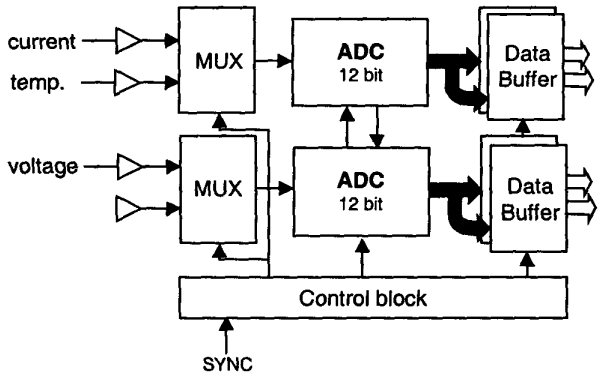

Fig. 8. Block diagram of data-acquisition subsystem

- Open and flexible communication protocol for distributed control of smart PEBBs
- Flexible, transparent and easy to use power modules
- Simple system integration and re-configuration.

The hardware design for the proposed controller is based upon the off-the-shelf components widely used in other engineering areas (especially in computers and communications), which brings us to conclude that the overall controller cost will be significantly reduced, regardless of the future smart module market.

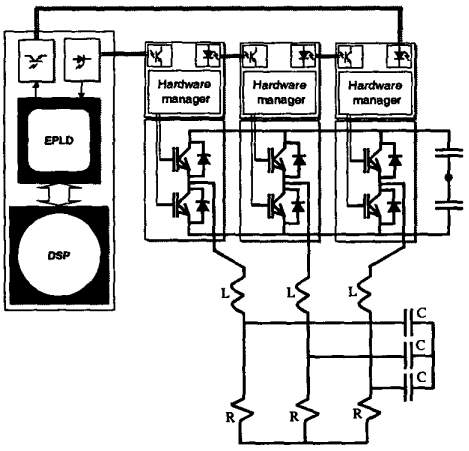

Fig. 9. Block diagram of experimental setup. (R=2.7 Ω, L=0.3 mH, C=600 μF)

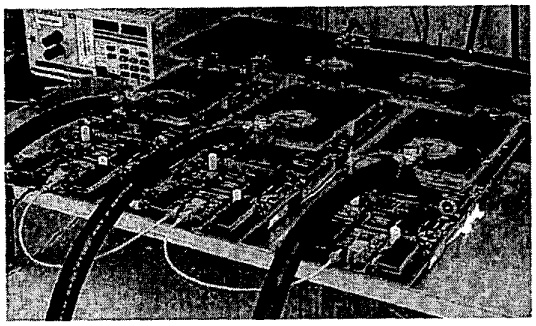

Fig. 10. Picture of a three-phase VSI designed following distributed controller concept.

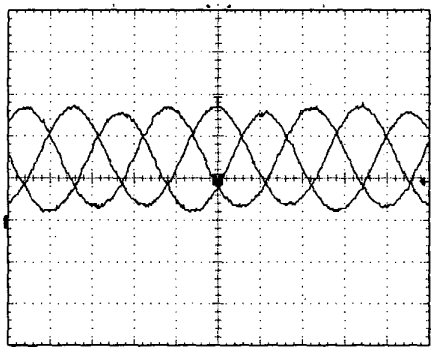

Fig. 11. Test waveforms showing converter output phase voltages. (100 V/div)

We believe that further optimization, and integration of the power stage with the hardware manager (using some of the advanced packaging techniques) will lead to a wide spectrum of reliable, compact, flexible and easy-to-use power processing units that will inevitably change power electronics design and practice. Additionally, as a result of the control partitioning, standard application control libraries can be established. Taken together, standard power modules, and software libraries would result in reduced non-recurring engineering cost, faster time to market and the economy of scale for medium and high power electronic applications.

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