A New Control Architecture for Future Distributed Power Electronics Systems

Ivan Celanovic, Nikola Celanovic, Ivana Milosavljevic[1], Dushan Boroyevich and Roger Cooley[2]

Center for Power Electronics Systems
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061-0111, USA

[1]Visteon Automotive Systems
17000 Rotunda Drive
Dearborn, MI 48121, USA

[2]Naval Surface Warfare Center,
Carderock Division, Electrical Systems Department
Philadelphia, PA 19112-5083, USA

Abstract–This paper proposes a novel open-architecture approach to the design of digital controller hardware for power electronics systems. The paper discusses the benefits of such an approach and compares it to the more conventional centralized controller approach. Prototypes of the three key open-architecture functional blocks: high-speed serial communication link, hardware manager and application manager were built in order to test their performance on a representative three-phase 100 kVA converter. Experimental results verify the feasibility of the proposed approach.

INTRODUCTION

Control of today's medium and high-power converters is, in most cases, based on a centralized digital controller, as explained in [1]. This approach has several drawbacks with perhaps the biggest one being the large number of point-to-point signal links that connect power stage and sensors on one side with the centralized controller on the other. Furthermore, the signals in typical power electronics systems come in variety of different formats and are transmitted through a variety of physical media. This makes the standardization and modularization of power electronics systems and subsystems very difficult, if not impossible.

In this paper we approach the issue of standardization in power electronics by standardizing the signal distribution network, which allows for open architecture distributed controller approach. The standardization of communication interface allows partitioning of power electronics system into flexible, easy-to-use, multifunctional modules or building blocks, which should significantly ease the task of system integration [2-4], [6-8]. Fig. 1 shows the functional diagram of an open architecture distributed controller approach suitable for application in power electronics systems.

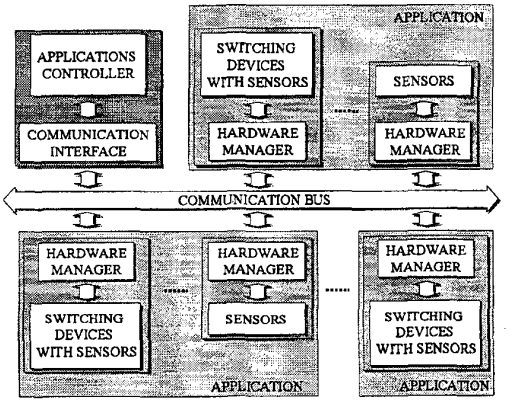

Fig. 1. Partitioning of power electronics system based on open-architecture distributed control approach.

The concept of a distributed controller is widely accepted in motion control and factory automation systems [9]. More along the lines of distributed control at the converter level was reported by Malapelle et al. [7] who proposed a distributed digital controller for high-power drives. They partitioned the system controller into a regulator and a bridge controller, which were connected via a relatively slow parallel bus. Toit et al. [6] have proposed a control structure where phase-leg controllers are connected to a higher-level controller through a (2.5 Mbits/sec) daisy-chained fiber optic link. In their structure the current control is implemented locally in a phase-leg controller, while the voltage control is implemented in a higher-level controller.

This paper proposes a real-time, digital control network suitable for medium- and high-power converters where the network communication protocol is designed to support modular and open-system design approach in power electronics.

This work was funded by the Office of Naval Research. This work made use of ERC Shared Facilities supported by the National Science Foundation under Award Number EEC-9731677

TABLE I
CONTROL NETWORK CHARACTERISTICS

Network	Speed	Max # of nodes	Arbitration	Cable type	Primary application
World FIP	31.2Kb/s, 1Mb/s, 2.5Mb/s	64 or 256	Bus Arbiter	Twisted pair, copper wire, optical fiber	Real-time control, Process/ machine
CAN	1 Mb/s	30	CSMA/CD enhanced	Twisted pair	Sensor/ actuators, automotive
Lon Works	Up to 1.25 Mb/s	32000	Predictive CSMA Collision Avoidance	Twisted pair, coaxial cable, fiber optic cable	Appliance control
SERCOS	2-4 Mb/s	256	Ring management	Plastic optical fiber	Motion control
MACRO	100 Mb/s	256	Ring management	Glass optical fiber, twisted pair	Motion control

In addition to the real-time control network this paper also introduces two new control architectural blocks that support proposed control network protocol and can be effectively used to form power electronics systems of various configurations. The architectural blocks in question are applications manager and hardware manager.

Following the proposed design paradigm the application manager liberated from any hardware-oriented tasks becomes universal and converter independent architectural block that can be configured to control any type of power electronics hardware, through the software only. At the same time, hardware manager designed as an integral part of either switching or sensing hardware, handles all the hardware specific tasks.

The partition of power electronics into proposed architectural blocks, we believe, also allows the development of a layered control software structure, with the hardware device drivers, libraries of standard control functions, and eventually with compilers from higher-level control design and simulation tools.

COMMUNICATION PROTOCOL

Because of the requirement of noise immunity, and in order to eliminate the large number of point to point links between the controller and the power the serial fiber optic ring network, like the one shown in Fig. 2 is chosen. The bit rate that this network needs to have can be found as a multiple of hardware managers in the network, number of bits per communicated word (including the control overhead bits) and converter switching frequency. Therefore, for a system with four nodes in the network, with ten twelve bit long words that need to be exchanged in every switching cycle and a fifty kilohertz switching frequency a channel capacity of about 36 Mbit/s is required. Furthermore, as shown in [5] the synchronization error between nodes should not exceed 0.1-0.2% of the switching frequency in order to eliminate low-frequency harmonics due to the synchronization.

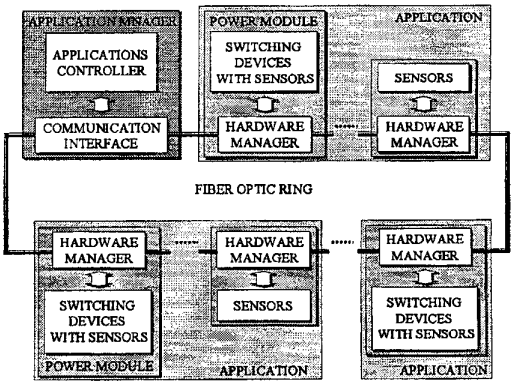

Fig. 2 Daisy-chained fiber optic control network for distributed control of power converters.

Because of those requirements none the five commercially available protocols designed for industrial control and automation applications that were considered for the application as power electronics were not found suitable.

Therefore, the communication network in this paper is designed as a master-slave ring network that runs over plastic 125 Mb/s fiber optic. In this type of network topology, application manager is a master node controlling the communications where all the hardware managers are operating in the slave mode.

A. Communication Protocol Functional Description

Master-slave protocol that is implemented insures deterministic response of the network. If the error occurs during transmission, corrupt data is not used. Instead the new data simply overwrites the previous data. This way the data flow is kept strictly predetermined.

Shown in Fig. 3 are two basic types of information communicated through the control network: time-critical data (exchanged in every switching cycle) and time non-critical data transmitted only after all the critical time variables have been passed to all nodes. Time-critical information include

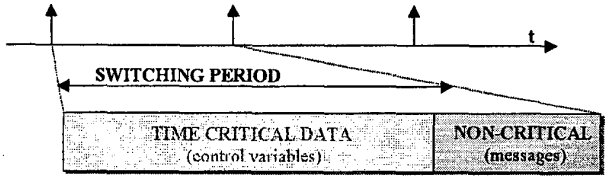

Fig. 3. Time allocation on the communications bus.

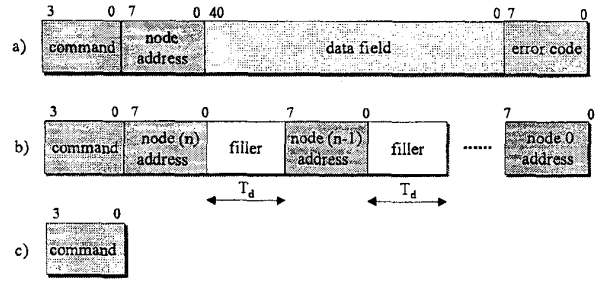

Fig. 4. Data formats in distributed controller network
a) data frame b) synchronization frame c) command frame

all the control variables such as: switching frequency information, duty cycle information and all the sensor information. Provision for non-critical data transfer is designed to support tasks such as initialization and software reconfiguration of the hardware managers. Non-critical data transfer is allowed only after all the time critical data is exchanged. Fig. 4 shows three types of time critical data frames: control data frame, synchronization frame and command frame.

The data frame consists of command indicating the beginning of the data packet, address of the node, data field and error check. The way data field is configured depends on the particular application and type of the hardware manager.

In a ring type of network, each node introduces a delay in data propagation path. Meaning that if we send synchronization command through the network, each node is going to receive the command with as many time delay T_d, as there are nodes between that node and the master node. The time delay, T_d, in the hardware test-bed implemented is typically around 460 ns. This means that the error in synchronization will generate time shifted PWM signals at the outputs, causing low frequency harmonics. This problem is solved with the synchronization sequence.

Format of the synchronization frame is shown in Fig. 4(b). The Frame starts with Synchronization command, and is followed by 8 bit long data blocks containing addresses of slave nodes and 'filler' fields, which are T_d long and are used for propagation delay compensation. The first address to be transmitted is of the slave node that is last to receive the frame. The number of address data blocks sent equals the number of slave nodes on the ring, which we want to synchronize. The first field is a synchronization command that alerts the nodes to wait for their time to synchronize. Next are the address fields of the nodes being synchronized. After the synchronization command is passed, the node awaits its address field. When the address is received, the node generates the synchronization signal. Because all the addresses are in reverse order and time delayed for the node propagation delay all the addresses will arrive at the destination nodes at almost the same time. Using this type of synchronization scheme in proposed 125 Mb/s fiber optical link synchronization error is reduced bellow 80 ns.

HARDWARE MANAGER DESIGN

Hardware manager in power electronics distributed network is designed to provide control and communication functions for the module it is associated with. It is designed to support all module specific control tasks thus making the module specific functions, such as for example soft switching, invisible to the applications manager. In the following sections two types of hardware managers will be discussed: a hardware manager for the power switching device, and a hardware manager for the current or voltage sensor.

A. Hardware Manager for Soft-Switched-Phase-Leg

The hardware manager shown in Fig. 5 is designed to control soft-switched phase leg. The following are the functions of this type of hardware manager:

- PWM generation for main and auxiliary switches;
- isolated gate drive for both main and auxiliary switches;
- over-current protection and indication;
- current, voltage and temperature sensing with A/D conversion; and
- communication of PWM, status and measurement information.

The only information the hardware manager communicates is a standardized serial data packet. All the necessary data for proper module operation are encoded in the data field of control data packet that was previously explained.

The hardware manager, shown in Fig. 5, consists of gate drives, a high speed ALTERA 10K PLD, two A/D converters, a high-speed ECL logic data transmitter and receiver, and a 125 Mbits/sec optical transceiver.

The communication interface within the hardware manager is built in three layers (according to ISO/OSI reduced reference model) defined as: physical layer, data link layer and application layer.

Physical layer is provided by means of an inexpensive plastic optic fiber, while interface between data link layer and physical layer is achieved using Hewlett Packard optical transceiver.

Data link layer is provided by TAXIchip™, (transmitter and receiver) [10]. An incoming optical signal is fed to the

transceiver and then to the TAXIchip™ [10] receiver. The receiver converts the serial stream into parallel, which is then loaded into the PLD for final data processing. Similarly, outgoing data from the PLD (in parallel form) are converted by the TAXIchip™ transmitter into a serial stream, amplified by the optical transceiver [11] and transmitted through the optical fiber.

The communication and control block, which is implemented in hardware (PLD), handles all application layer functions. The communication and control subsystem can be viewed as a state machine, shown in Fig. 6, receiving commands through the network and changing states and outputs accordingly. Its basic states are described as:

- idle mode (waiting for the data packet to arrive),
- forward mode (passing the information to the subsequent node),
- active mode (incoming data packet has the address of the node): when the data is being first verified by CRC checker and then stored in corresponding buffers and the packet is then forwarded with the results of current/voltage/temperature measurements and local status information,
- synchronization mode (after receiving SYNC command from application manager): which reloads the double buffers, initiates A/D conversion and resets PWM generator and
- initialization mode: which initializes the whole system and dynamically assigns the node address.

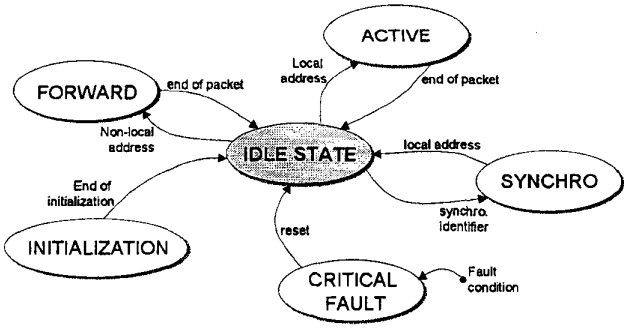

Fig. 6. State transition diagram for communication controller.

PWM generator and local fault protection are also realized in the PLD. Three main parameters necessary for proper operation of PWM generator are: duty cycle, switching period and the synchronization command. The duty cycle data, when received and validated for proper transmission, are stored in the input buffer. The duty cycle becomes active only after it receives synchronization command from the application manager, which moves the duty cycle information to executable buffer used for PWM generation. Period information (which controls switching frequency of the leg) is also double-buffered for the sake of proper synchronization. A digital comparator compares the content

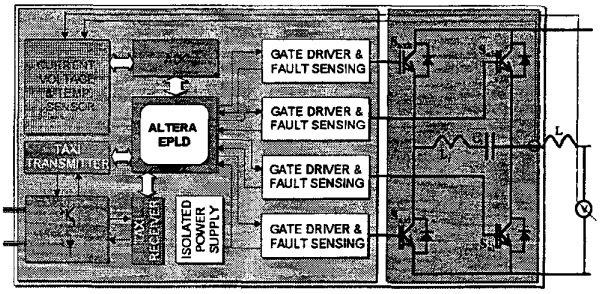

Fig. 5. Block diagram of designed hardware manager controlling soft-switched phase leg.

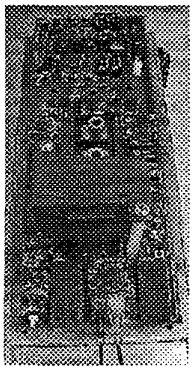

Fig. 7. Prototype of phase leg module integrated with hardware manager.

of the counter with duty cycle creating a control pulse for the switch. The dead time generator and fault protection are the final stages in PWM generation, providing shoot-through and over current/voltage/temperature protection.

Most of today's control systems in power electronics are based on full-state feedback, which requires per-switching cycle current and voltage measurement. Therefore, the designed hardware manager consists of current, voltage and temperature sensors. Measurement of module voltage and current is performed simultaneously per switching cycle using two 12-bits AD converters, while temperature measurement is performed with 10 times slower rate. Proper timing is achieved also through synchronization command received from application manager. Measurement results are stored in the output buffer, ready to be packed into a corresponding data packet and sent to applications manager.

B. Hardware Manger for Distributed Sensor

Although the hardware manager has built-in current, voltage and temperature sensors for some applications, additional system sensors such as position, velocity etc. are needed to provide feedback to the application controller. To overcome this limitation a new architectural block smart sensor is introduced. It is designed to follow the same communication protocol, has a built in A/D converter and sensor and same communication interface as smart module. Fig. 8 shows the functional diagram and the hardware

prototype of the smart sensor. The instants of A/D conversion are synchronized with the rest of the network using the already explained synchronization frame.

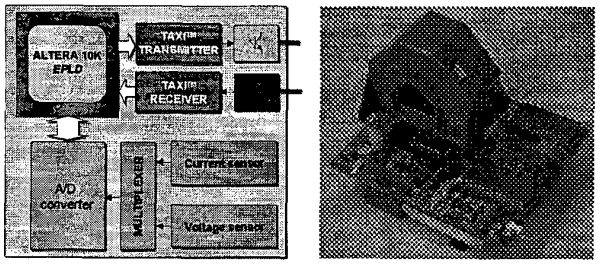

Fig. 8. Block diagram and hardware prototype of the distributed current sensor.

APPLICATIONS MANAGER

The application manager, is a high-level controller liberated from low-level hardware oriented tasks. It is designed to provide the system with flexibility and software reconfigurability.

The prototype application manager (Fig. 9) is built around Analog Devices 21062 SHARC floating point DSP processor, with an onboard ALTERA 10K PLD and fiber-optic communication interface that provides open control architecture capable of controlling multiple independent modules. This allows the applications manager hardware architecture to be independent of the converter topology, number of switches, sensors, etc. and allows system reconfiguration through software only.

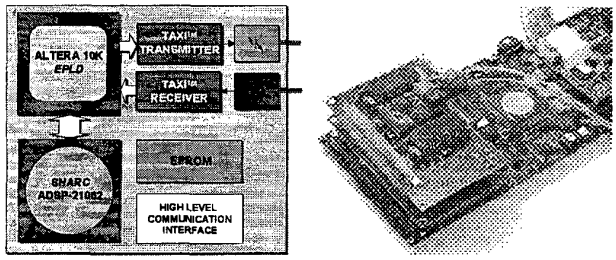

Fig. 9. Block diagram and application manager hardware prototype.

EXPERIMENTAL RESULTS

To verify the idea of a distributed controller, a three-phase voltage source inverter (VSI) driving a simple R-L load was designed as shown in Fig. 10. Prototype of the converter consists of three smart hardware managers controlling soft-switched phase leg modules, connected via fiber optic communication link, while the application manager performs control tasks related to controlling the output currents of the inverter in closed-loop manner.

Each phase leg is designed using 1200 V, 300 A IGBT phase-leg modules as main switches. Fig 12 shows output current waveforms of the three-phase VSI with the closed current loops in DQ reference frame.

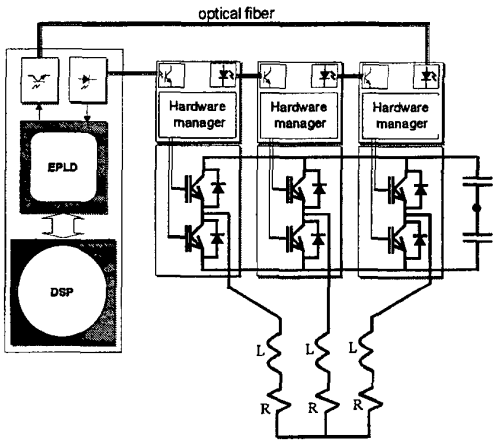

Fig. 10. Block diagram of three-phase VSI built using distributed control approach.

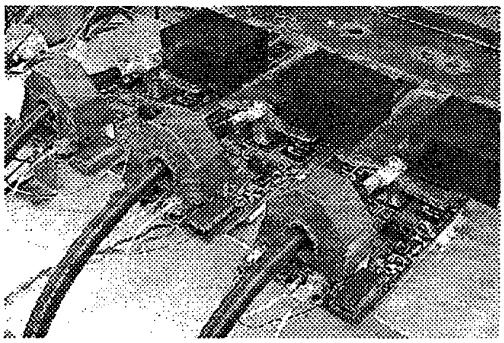

Fig.11. Prototype three-phase VSI built using smart modules and distributed controller approach.

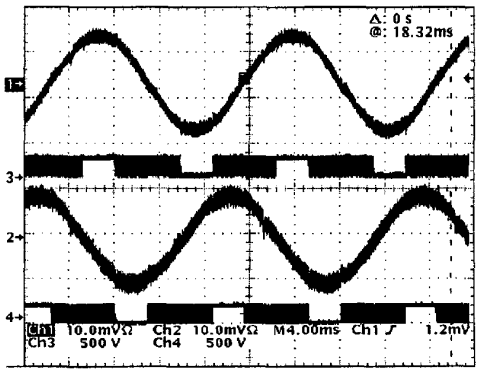

Fig. 12. Output phase currents (50 A/div) and output phase voltages (500 V/div) PWM waveforms.

CONCLUSION

This paper presented a novel approach to power electronics system design based on the open architecture distributed digital controller and modular power electronics building blocks. The most important features of the new concept are:

- Open and flexible communication protocol for distributed control of power electronics systems;
- Flexible, and easy to use power converter modules;
- Hardware independent, applications manager capable of controlling several different types of converters in parallel, and
- Simple system integration and re-configuration.

We believe that distributed digital controller environment together with open-system communication protocol provides solid ground for object oriented software design in power electronics. This will also enable easier integration of higher-level graphically oriented design and simulation tools with power electronics hardware.

Finally, we anticipate that both hardware and software standardization and modularization will lead to user friendly, plug and play, system oriented design in power electronics as opposed to today's predominantly circuit oriented, custom design practice.

ACKNOWLEDGMENT

Authors would like to thank the Office of Naval Research for their vision of the Power Electronics Building Block.

REFERENCES

[1] V. Vlatkovic, and D. Borojevic, "Digital-Signal-Processor-Based Control of Three-Phase Space Vector Modulated Converters," *IEEE Transactions on Industrial Electronics*, June 1994, Vol. 41, No. 3, pp. 326-332.

[2] T. Ericsen, A. Tucker, "Power Electronics Building Blocks and Potential Power Modulator Applications," *IEEE Conference Record of the Twenty-Third International Power Modulator Symposium*, New York, NY, 1998, pp. 12-15.

[3] Van Wyk, F.C. Lee, "Power Electronics Technology at the Dawn the New Millennium-Status and Future," *IEEE PESC Conference Proceedings*, 1999.

[4] I. Celanovic, I. Milosavljevic, D. Boroyevich, G. Jinhong, R. Cooley, "A New Distributed Controller for the Next Generation Power Electronics Building Blocks," 15th Annual *IEEE Applied Power Electronics Conference Proceedings*, February 2000, pp. 889-894.

[5] I. Milosavljevic, Z. Ye, D. Borojevic, C. Holton, "Analysis of Converter Operation with a Phase-Leg in Daisy-Chained or Ring Type Structure," *IEEE PESC Conference Proceedings*, June 1999.

[6] J.A. Du Toit, A.D. Le Roux, J.H.R. Enslin, "An Integrated Controller Module for Distributed Control of Power Electronics," *IEEE APEC '98 Proceedings*, February 1998, pp. 874-880.

[7] P.L.G. Malapelle, G. Torri, R. Moruzzi, A. Oliva, "A New, Modular, Programmable, High Speed Digital Control for Large Drives," *IEEE IECON 20th International Conference on Industrial Electronics, Control and Instrumentation*, 1994; vol.1, pp. p.210-14.

[8] I Milosavljevic, D., Borojevic., I. Celanovic, "Modularized Communication and Control Structure for Power Converters," *8th European Conference on Power Electronics and Applications, EPE*, September 1999.

[9] E. Bassi, F. Benzi, L. Lusetti, G.S. Buja, "Communication Protocols for Electrical Drives," *IEEE IECON Proceedings, 1995*, Vol. 2, pp.706-711.

[10] "TAXIchip™ Integrated Circuits," *Data Sheet and Technical Manual, Publication#07370*, AMD, April 1994.

[11] "Plastic Optical Fiber and HCS® Fiber Cable and Connectors for Versatile Link," *Technical Data 5963-3711E*, Hewlett Packard, November 1994.