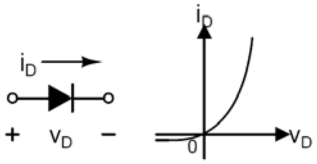
VIII. DIODES

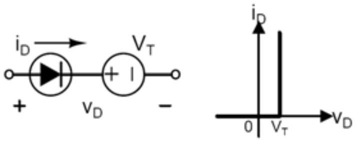
→ Passive devices that only pass current in one direction

- **Shockley Diode Equation**: $i_D = I_S\left(e^{v_D/V_{th}} - 1\right)$

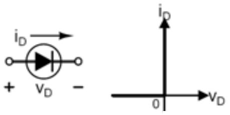
  I_S = reverse-bias saturation current (~10^{-12} A for Silicon)
  $V_{th} = k_B T/q$ = thermal voltage (~26mV @ room temp T=300K)



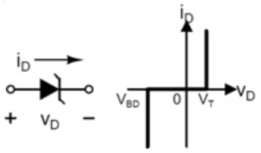
- **Large-Signal Diode Model** (simplifies circuit analysis)
  2 states: ◦ "on" – forward bias ($v_D = V_T$): $i_D \geq 0$
  ◦ "off" – reverse bias ($v_D < V_T$): $i_D = 0$
  V_T = threshold voltage ~ 0.6V



- **Ideal Diode Model (Perfect Rectifier)**
  → large-signal diode model with $V_T = 0$

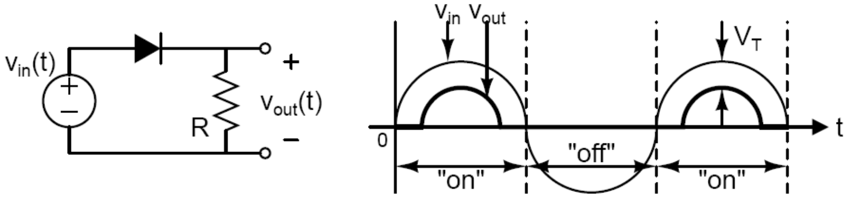


- **Zener Diode (simplified)**
  3 states: ◦ forward bias: $v_D = V_T$, $i_D \geq 0$
  ◦ reverse bias: $V_{BD} < v_D < V_T$, $i_D = 0$
  ◦ breakdown: $v_D = V_{BD}$, $i_D \leq 0$

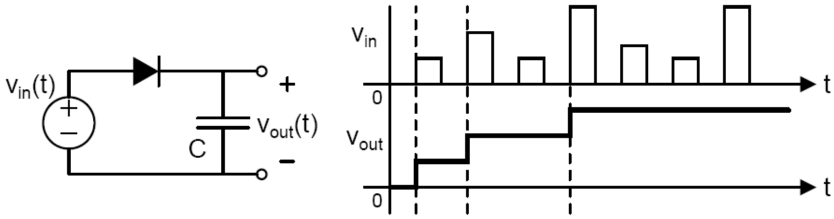


- **Diode Circuit Analysis – Method of Assumed States**
  (1) Guess the state of each diode (on or off). For large-signal diode model, replace "on" diodes with voltage source with voltage drop V_T and "off" diodes with open circuits.
  (2) Solve the circuit using KCL/KVL.
  (3) Check if assumptions for diode states were correct (i.e., check that "on" diodes have $i_D \geq 0$ and "off" diodes have $v_D < V_T$). If not, start over, guessing new states for the diodes.

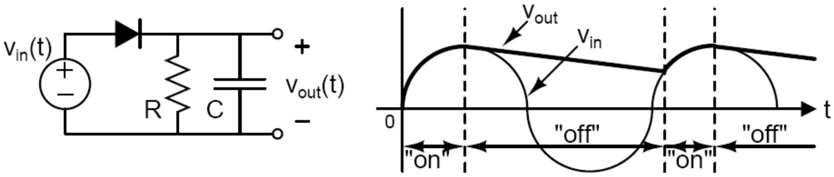
- **Rectifier Circuit**



- **Peak Detector Circuit** (V_T=0)



- **AC-DC Converter** (V_T=0)



IX. MOSFET

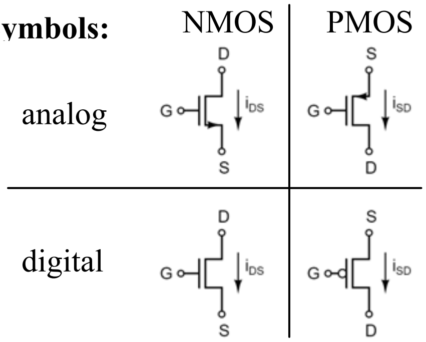
Metal Oxide Semiconductor Field Effect Transistor

(transistor – a 3+ terminal device in which one terminal controls the current flow between the other two terminals)

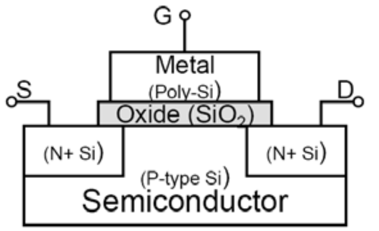
→ For a MOSFET, the gate controls the current flow between source and drain.

- ◦ For an n-channel MOSFET (NMOS), a positive gate voltage produces current flow
- ◦ For a p-channel MOSFET (PMOS), a negative gate voltage produces current flow

Circuit Symbols:



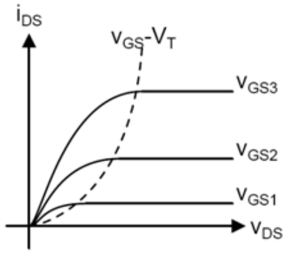
NMOS Physical Structure:



- **NMOS IV Characteristic – Square Law Model**

  3 regions of operation:

cutoff	$V_{GS} < V_{Tn}$	$I_{DS} = 0$
triode/linear	$V_{GS} > V_{Tn}$ $V_{DS} \leq V_{GS} - V_{Tn}$	$I_{DS} = K_n(V_{GS}-V_{Tn}-V_{DS}/2)V_{DS}$
saturation	$V_{GS} > V_{Tn}$ $V_{DS} \geq V_{GS} - V_{Tn}$	$I_{DSAT} = ½K_n(V_{GS}-V_{Tn})^2$



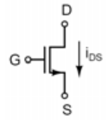
$V_{GS} = V_G – V_S$, $V_{DS} = V_D – V_S$

V_{Tn} = threshold voltage (NMOS)

$V_{DSAT} = V_{GS} - V_{Tn}$ = saturation voltage

I_{DSAT} = saturation current

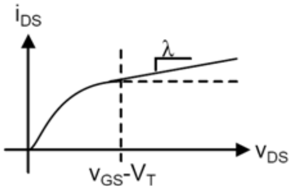
K_n = constant determined by manufacturing process and transistor size (units: A/V^2)



- **Channel-Length Modulation Parameter λ**

  → In the saturation region, I_{DS} is not perfectly constant for all $V_{DS} \geq V_{DSAT}$; as V_{DS} increases, I_{DS} also increases. An additional factor $(1+\lambda V_{DS})$ in the IV equation models this effect (the factor is also added to the triode equation to make the IV curve continuous):

cutoff	$V_{GS} < V_{Tn}$	$I_{DS} = 0$
triode/linear	$V_{GS} > V_{Tn}$ $V_{DS} \leq V_{DSAT}$	$I_{DS} = K_n(V_{GS}-V_{Tn}-V_{DS}/2)V_{DS}(1+\lambda_n V_{DS})$
saturation	$V_{GS} > V_{Tn}$ $V_{DS} \geq V_{DSAT}$	$I_{DS} = ½K_n(V_{GS}-V_{Tn})^2(1+\lambda_n V_{DS})$



- **PMOS IV Characteristic – Square Law Model**

  → Same as NMOS, but switch polarity for everything (V_{Tp} is typically negative)

cutoff	$V_{SG} < -V_{Tp}$	$I_{SD} = 0$
triode/linear	$V_{SG} > -V_{Tp}$ $V_{SD} \leq V_{SG} + V_{Tp}$	$I_{SD} = K_p(V_{SG}+V_{Tp}-V_{SD}/2)V_{SD}(1+\lambda_p V_{SD})$
saturation	$V_{SG} > -V_{Tp}$ $V_{SD} \geq V_{SG} + V_{Tp}$	$I_{SD} = ½K_p(V_{SG}+V_{Tp})^2(1+\lambda_p V_{SD})$