I have neither given nor received aid on this homework, nor have I concealed any violations of the honor code.

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Introduction

The purpose of this project is to design, build and test a multi-stage amplifier circuit that might be used for audio amplification. Audio equipment is one of the most important uses of analog circuit design.

The design has to meet several specifications that a real audio amplifier might be required to have. Its frequency response should be limited to what is audible to the human ear (50Hz-23kHz), must have a gain of 3500, power consumption should be less than 300mW while providing an output of 2V peak-to-peak, input impedance should be at least 100k\(\Omega\) and the output impedance should be less than 25\(\Omega\).

As we have seen in the previous project, performances of single stage amplifiers are severely limited and real life applications almost always require multi-stage designs. For this design a three-stage layout using four NPN type 2N2904 transistors were used, using same transistors makes design calculations a little easier and reduces the number of steps required for solid state integrated circuit production.

The first stage is a Darlington pair that provides very high input impedance and most of the voltage gain. Second stage is a single transistor used in common emitter with degeneracy configuration, it provides some gain and gives us the high cut-off frequency we need. The third and final stage is an emitter follower to provide low output impedance, so our circuit can provide a lot of current to the load.

Since we were concerned only with the small signal response, both the input and output are AC coupled. Another coupling capacitor used between the first and second stages so we can have both stages at the desired biasing points without worrying about the other.

Design Strategy

Design Order

There are multiple difficulties inherent in this design that made the design process difficult to carry out in a completely linear fashion. With only five capacitors to use, some stages need to be DC coupled, so DC bias design cannot be completely separated into stages. Also, the amplification of each stage depends on the input and output resistances of the preceding and following stages, so the AC analysis is difficult to separate. The work required to derive a transfer equation for the entire four-transistor amplifier by hand is rather large. Therefore, we chose to follow a non-linear design approach similar to the one suggested in the lab manual where we use Accusim simultaneously with hand design to verify and check our results and equations. Using this method, we setup our DC bias equations by hand and then checked if they were valid in Accusim. Next we could hand design for gain and return to Accusim to check the validity of our gain equations. Using this segmented design strategy, we were sure that our hand design calculations were valid.

Initial Design

For our first design, we chose to follow the architecture suggested in the lab manual and to use DC coupling between all stages. The architecture recommended was: emitter follower, common emitter, common emitter with degeneracy, and emitter follower. Although DC
coupling makes the bias point selection more difficult, it does reduce the number of components needed by using only one resistor bias ladder. By eliminating extra bias ladders, we also can theoretically increase gain, as signal would normally be attenuated in these chains. DC coupling also allows us to use the five capacitors wherever we need elsewhere in the circuit, such as for bypass and input/output coupling.

Design Trial 1

Because the DC and AC parameters are linked across the stages, we found it advantageous to use a computer spreadsheet program (Microsoft Excel) to help us select resistor values. We could then easily change one single value and have it propagate through all the equations saving hours of manual hand calculations. We also wrote the spreadsheet to easily calculate the small signal parameters ($g_m$, $r_p$, $r_o$) for each transistor as well.

In the first trial, the required bias ladder on the input pulled the input resistance low, so a series input resistor was added. Although this simplified meeting the input resistance specification, it severely attenuated the signal, so we eliminated the use of emitter degeneracy on the third stage. Other problems we had included very high output resistance, and some significant sensitivity to current gain parameters of the transistors.

Alternate Architecture – The Darlington Pair

What we really wanted to do was to simplify the analysis by separating the sections with a coupling capacitor. The ideal place to break the amplifier up is between the second and third stages (the amplification stages) because the gains of these two stages are closely tied to the DC bias conditions. The first stage existed only to provide a high input resistance mainly through emitter resistance multiplication. However, the collector current and therefore base current had to be small in order to meet the conflicting requirements for beta insensitivity and high bias resistance. This was especially important because we didn’t want to use and input series resistance to artificially increase $R_{IN}$. If $I_C$ decreases and $R_E$ increases significantly, the problems with input resistance and losing signal are eliminated in the first stage but the output resistance is driven abnormally high and the base current of the second stage cannot be maintained.

However, if the emitter of the first stage is connected directly to the base of the second stage, this eliminates the problems with output resistance and DC bias point. If we finally connect the two collectors together, we have created a Darlington pair. A Darlington pair can be treated as one transistor with a current gain that is the product of the current gains of two
transistors. The composite small signal parameters are also easy to derive. By using the Darlington pair as a composite first stage in the amplifier, the total number of stages is reduced to three. The because of the extremely high effective current gain of the pair, a nominal collector current can require only a very small base current and therefore a high resistance bias ladder. Furthermore, with the arrangement yields a very high input impedance because the emitter multiplication factor is applied twice. Even with no emitter degeneracy the $r_{p2}$ resistance is still multiplied by $Q_1$ and with $I_{C1}$ so small, $r_{p1}$ is very high. Therefore, the composite stage is operated as a common emitter amplifier with extremely high input resistance.

With the bias constraints of the first stage removed from the rest of the circuit, we focused on the final gain and output stages (2 & 3). It seemed that in order to get maximum output swing and minimize output resistance, the collector resistor on the output emitter follower was unnecessary. We also chose to use all NPN transistors for consistency and because we no longer needed to worry about the DC bias point conditions between the two voltage amplifiers. By capacitively coupling the first and second stages, it was necessary to add a second bias ladder. However, we could use raw gain to overcome the loss in output signal due to the added loading on the first stage. Knowing we would probably have to reduce the gain slightly in the second stage, we included emitter degeneracy in the second stage using a split emitter resistor setup where $R_{E2}=R_{E2a}+R_{E2b}$. The final circuit diagram is on the following page.

**Parameter Selections**

With the new circuit architecture, the spreadsheet had to be rewritten, but it used basically the same techniques. Furthermore, we expanded the spreadsheet to include calculating the $R_{IN}$, $R_{OUT}$ and $A_V$ parameters of the amplifier. For the hand calculations and the simulations, we used current gain of 150 and 170 and an Early voltage of $-171V$. Because we are trying to design for reasonable bias stability and insensitivity to beta, it was felt that measuring beta for each transistor would be unnecessary if we designed our circuit correctly. We used a current gain of $\beta=170$ for the transistor we reused from Lab 5 and $\beta=150$ as an average of possible values for other transistors. The Early voltage is what we measured in Lab 5. The following table is a guide to pick values:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Stage 1: CE</th>
<th>Stage 2: CE+D.</th>
<th>Stage 3: CC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>~100</td>
<td>~40</td>
<td>~1</td>
</tr>
<tr>
<td>$I_C$</td>
<td>1mA</td>
<td>0.5mA</td>
<td>15mA</td>
</tr>
<tr>
<td>Input R</td>
<td>&gt;1MO</td>
<td>$&gt;R_{OUT1}$</td>
<td>$&gt;R_{OUT2}$</td>
</tr>
<tr>
<td>Output Swing</td>
<td>50mV</td>
<td>~2V ppk</td>
<td>2V ppk</td>
</tr>
</tbody>
</table>

The circuit topology in the lab manual suggests using two gain stages with significantly different voltage gains. However, from our experience with Lab 5, making a common emitter amplifier with a very high or rather low gain is difficult because of the limitations of the circuit or the transistor. We felt it was better to aim for gains that were more middle-of-the-road. The collector current in the first stage was chosen to be a moderate value low enough to keep the bias ladder requirements low. The second stage has a low current for the same reason, to keep the
bias ladder resistance high. Stage 3 is only an emitter follower with a gain slightly less than one. Therefore, the $2V_{ppk}$ output voltage swing must be developed by stage 2. In order to meet the low output resistance and be able to drive a high capacitance load, the current in the last stage is relatively high and accounts for 90% of the power supply current draw. In order not to lose too much of our signal from impedance mismatch, we chose the input resistance of each stage to be greater than or equal to the output resistance of the preceding stage.

Also of concern to the design are the collector to emitter and the emitter voltages. We found in Lab 5 that having an emitter voltage between about 1.6V to 2V was a good range for reducing sensitivity to changes in current gain. We also found from our hand calculations that the raw voltage gain of a common emitter amplifier was dependent on the voltage over the collector resistor, or therefore inversely proportional to $V_{CE}$. In Lab 5, we used a $V_{CE}$ of 2V for a gain of 160. Therefore, we choose $V_{CE2}$~5V and $V_{CE3}$~6V as a starting point to look at for the two voltage amplifier stages. $V_{CE2}$ has to be high anyway to keep $Q_1$ properly biased in the Darlington Pair

The AC Analysis of the three stage amplifier is much more complex than a single stage amplifier. For determining the upper and lower cutoff frequencies, the Open Circuit Time Constant and Short Circuit Time Constant methods could be used. However, these require pages and pages of calculations. A less rigorous approach may not be as accurate, but it will be faster to get to simulation. Then in simulation, any errors can be corrected.

For the high frequency cutoff frequency, we will assume that the compensation capacitor and $C_{\mu3}$ is the dominant pole. However, in simulation we saw that our first estimation of the cutoff frequency was about half of the simulated cutoff frequency so we reincorporated this factor into our hand calculation equation. For the low frequency cutoff, we also used an estimation technique to meet the requirement. Instead of calculating the SCTC frequency, we tried to make the capacitive reactance at the maximum $f_L$ much smaller than the approximate resistance seen by the capacitor. By doing this, we can guarantee meeting the specifications, even if it doesn’t calculate the exact lower cutoff frequency.

The last step was to check our peak output voltage swing. In this case, our second stage with $Q_3$ is going to be our limiting stage, so we need to make sure that $V_{p3}$ does not go over 10m$V_{pk}$. By using the resistance reflection rule and the voltage gain of this stage, we were able to calculate the peak output voltage.
\[
\begin{align*}
V_{E1} &= \frac{V_{EE} \cdot R_E}{R_{b1} + R_{b2}} \\
V_{E2} &= V_{E1} \neq 1.4V \\
K_{bb} &= \frac{R_{b1} \parallel R_{b2}}{R_{b1} + R_{b2}} \\
K_{bb} &= \frac{R_{b1} \cdot R_{b2}}{R_{b1} + R_{b2}} \\
V_{bb} &= I_3, K_{bb} = 1.4V - B_1 B_2 I_{b1}, R_{E} = 0 \\
I_{E1} &= \frac{V_{bb} - 1.4V}{R_{bb} + B_2 B_1 R_E} \\
I_{E2} &= I_{E1} + I_{E2} = B_1 B_2 I_{b1} \\
V_{E1} &= I_{E1} \cdot R_{E} \\
V_{E2} &= V_{E1} + V_{E2} \\
\frac{V_{EE} - V_{E1}}{I_{E1}} &= R_{E1}
\end{align*}
\]

\[
\begin{align*}
\Gamma &= \frac{\sigma_{m3}}{2} = \frac{\sigma_{m2}}{2V_f} = 20 B_2 (B_1 + 1) I_{b1} \\
\Gamma &= \Gamma_1 + \Gamma_2 (1 + B_2) = \frac{1}{20 B_2} + \frac{B_2}{20 B_2} = \frac{1}{20 B_2}
\end{align*}
\]

\[
\begin{align*}
V_{bb} &= \frac{V_{E1} \cdot R_{b1}}{R_{b1} + R_{b2}} \\
K_{bb} &= \frac{R_{b1} \cdot R_{b2}}{R_{b1} + R_{b2}} \\
I_{b2} &= \frac{V_{bb} - 0.7}{R_{b1} + (1 + B_2) R_E} \\
I_{E2} &= \frac{V_{E2}}{R_{b1}} \\
I_{E2} &= V_{E2} - V_{E4} = V_{E4} + 0.7
\end{align*}
\]

\[
\begin{align*}
\sigma_{m2} &= 40 I_{b1} \\
\Gamma_3 &= \frac{B_2}{I_{b2}} \\
\Gamma_4 &= \frac{B_2}{I_{b4}} \\
\Gamma &= \frac{1}{\sigma_{m2}} \\
\Gamma &= \frac{1}{\sigma_{m2}} \\
R_{out} &= \frac{R_{E2} \parallel (\Gamma_{m2} + \frac{R_{E2} \Gamma_{m2}}{\Gamma_{m2}} + \Gamma)}{R_{E2} + \Gamma} \\
I_{b1} &= \frac{V_{E1}}{R_{b1} + R_{b2}} \\
I_{b2} &= \frac{V_{E2}}{R_{b1} + R_{b2}} \\
I_{b3} &= I_{E1} + I_{E2} + I_{E4} + I_{E4} + I_{b1} + I_{b2}
\end{align*}
\]
### Lab 6: Bias Point Matrix

**FINAL ITERATION W/ DARLINGTON PAIR**

<table>
<thead>
<tr>
<th>Q-Point Choices</th>
<th>Bias Points</th>
<th>Small Sig Params</th>
<th>Amplifier Params</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc: 12 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_Load 200 Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_source 4.00E+03 Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q' (Q1 &amp; Q2)</th>
<th><strong>NPN - CE Darlington Stage</strong></th>
<th>For Voltage gain and high input impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beta 1: 174</td>
<td>V_BB1~ 3.2</td>
<td>Vth: 9.90E-01</td>
</tr>
<tr>
<td>V_A1: 171</td>
<td>R_B1~ 1.46E+06 gm': 0.020115</td>
<td>Rth: 3.96E+03</td>
</tr>
<tr>
<td>Beta 2: 174</td>
<td>R_B2~ 5.32E+05 r_pi' 1.51E+06</td>
<td></td>
</tr>
<tr>
<td>V_A2: 171</td>
<td>I_Bias1: 6.02E-06 r_o' 1.17E+05 RL2': 3.53E+03 ro2//RC1//RBB2/RIN3</td>
<td></td>
</tr>
<tr>
<td>V_CE2: 5 V</td>
<td>R_E1~ 1.80E+03 R_IN 3.10E+05</td>
<td></td>
</tr>
<tr>
<td>I_C2: 1.00E-03 A</td>
<td>R_C1~ 5.20E+03</td>
<td>ROUT' 4.98E+03</td>
</tr>
<tr>
<td>R_BB1: 3.90E+05 Ω</td>
<td></td>
<td>V_OPPK -2.06E+00</td>
</tr>
<tr>
<td>V_E': 1.8 V</td>
<td>I_B1~ 3.303E-08</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q3:</th>
<th><strong>NPN - CE with possible degener</strong></th>
<th>For Voltage Gain and DC bias for Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beta 3: 150</td>
<td>V_BB2~ 2.5</td>
<td>RIN2: 1.59E+04</td>
</tr>
<tr>
<td>V_A3: 171</td>
<td>R_B3~ 2.47E+05 gm3: 1.80E-02</td>
<td>RL2': 5.71E+03</td>
</tr>
<tr>
<td>V_CE3: xxxxxxxx</td>
<td>I_Bias2: 3.84E-05 r_o3: 3.94E+05</td>
<td>Rth2': 4.54E+03</td>
</tr>
<tr>
<td>I_C3: 4.50E-04 A</td>
<td>I_B3~ 3.00E-06 R_B4~ 6.51E+04 r_pi3: 8.33E+03</td>
<td>ROUT2/RBB2</td>
</tr>
<tr>
<td>V_E3: 1.62 V</td>
<td>R_E2~ 3.60E+03</td>
<td>AVth2: -5.41E+01</td>
</tr>
<tr>
<td>R_BB2: 5.15E+04 O</td>
<td>R_E2a: 5.00E+01 I_B3~ 3.00E-06</td>
<td>ROUT2: 7.83E+03</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q4:</th>
<th><strong>NPN - CC</strong></th>
<th>For driving output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beta 4: 150</td>
<td>R_E3: 5.00E+02</td>
<td>R_L: 1.41E+02 ro4//R_L//RE4</td>
</tr>
<tr>
<td>V_A4: 171</td>
<td>V_CE4: 5 gm4: 5.60E-01</td>
<td>Rth3: 7.83E+03 ROUT3</td>
</tr>
<tr>
<td>I_C4: 1.40E-02 A</td>
<td>I_B4: 9.33E-05 r_o4: 1.26E+04</td>
<td>RIN3: 2.16E+04</td>
</tr>
<tr>
<td>V_E4: 7 V</td>
<td>V_CE3: 6.08 r_e4: 1.79E+00</td>
<td>AVth3: 9.88E-01</td>
</tr>
<tr>
<td>Vpi_lin_limit 1.00E-02 Vpk</td>
<td>I_R_C3: 5.43E-04 R_C2: 7.91E+03</td>
<td>re+Rout2/(B+1) 5.36E+01</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>---</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>1</td>
<td>Lab 6: Bias Point Matrix</td>
<td>FINAL ITERATION W/ DARLINGTON PAIR</td>
</tr>
<tr>
<td>5</td>
<td>Vcc: 12 V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>R_Load 200 Ω</td>
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<tr>
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<td></td>
</tr>
<tr>
<td>9</td>
<td>Q’ (Q1 &amp; Q2)</td>
<td>NPN - CE Darlington Stage</td>
</tr>
<tr>
<td>11</td>
<td>V_A1: 171</td>
<td>R_B1~</td>
</tr>
<tr>
<td>12</td>
<td>Beta 2: 174</td>
<td>R_B2~</td>
</tr>
<tr>
<td>13</td>
<td>V_A2: 171</td>
<td>I_Bias1:</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>I_B1~</td>
</tr>
<tr>
<td>15</td>
<td>V_CE2: 5 V</td>
<td>R_E1~</td>
</tr>
<tr>
<td>16</td>
<td>I_C2: 1.00E-03 A</td>
<td>R_C1~</td>
</tr>
<tr>
<td>17</td>
<td>R_BB1: 3.90E+05 Ω</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>V_E': 1.8 V</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Q3: NPN - CE with possible degen.</td>
<td>For Voltage Gain and DC bias for Q4</td>
</tr>
<tr>
<td>22</td>
<td>V_A3: 171</td>
<td>R_B3~</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>R_B4~</td>
</tr>
<tr>
<td>24</td>
<td>V_CE3: \text{xxxxxxx}</td>
<td>I_Bias2:</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>I_C3: 4.50E-04 A</td>
</tr>
<tr>
<td>27</td>
<td>R_BB2: 5.15E+04 Ω</td>
<td>R_E2a:</td>
</tr>
<tr>
<td>29</td>
<td>Q4: NPN - CC</td>
<td>For driving output</td>
</tr>
<tr>
<td>31</td>
<td>V_A4: 171</td>
<td>V_CE4:</td>
</tr>
<tr>
<td>33</td>
<td>I_C4: 1.40E-02 A</td>
<td>I_B4:</td>
</tr>
<tr>
<td>34</td>
<td>V_E4: 7 V</td>
<td>r_e4:</td>
</tr>
<tr>
<td>35</td>
<td>V_CE3: =F32-B26</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>Vpi_lin_limit 1.00E-02 Vpk</td>
<td>I_R_C3:</td>
</tr>
<tr>
<td>37</td>
<td>R_C2:</td>
<td>=B5-F32/F36</td>
</tr>
</tbody>
</table>
AC Analysis: High Frequency Cutoff

- Assume $C_{in}$ is dominant pole (in parallel with $G_{m3}$) but not only high frequency effect

$$\frac{V_{in}}{V_{in}} = R_{in} = \frac{R_{in}}{R_{in} + R_C}$$

$$\frac{V_{out}}{V_{in}} = V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_C}{R_C + R_L}$$

Use eqn. 17.110 from book when $R_{in}$ is small.

$$R_L = R_L' + R_{in} \frac{1}{\left( \left( \frac{G_{m3}}{G_{m3} + (B)} \right) R_C \right)} \left( 1 + \frac{R_C}{R_L} \right)$$

$$\text{because of simplification, we expect this to overestimate $$f_H$$ as with CTCE.}$$

$$\text{we arbitrarily assume our simplification overestimates by a factor of 2.}$$

$$f_H = \left[ \frac{1}{\left( \frac{1}{C_{in} + C_C} \right) \left( \frac{R_L' + R_{in} \frac{1}{\left( \left( \frac{G_{m3}}{G_{m3} + (B)} \right) R_C \right)} \left( 1 + \frac{R_C}{R_L} \right) \right) \left( 1 + \frac{B R_L'}{G_{m3} + R_L'\left( \frac{G_{m3}}{G_{m3} + (B)} \right) R_C \right) \right]^{-1}$$

- Could do STC method

- Instead use equivalent capacitive resistance where

$$X_C = \frac{1}{2\pi f_C}$$

So make $X_C \ll R_L'$ where $R_L'$ is approximate resistance of circuit and select $f_C$ at desired low frequency cutoff or approximately

$$C_C > \frac{1}{2\pi f_C X_C}$$
HF:

\[ R_{1}^{1} = 5.79\,k\Omega \quad R_{p} = 575.36\,k\Omega \]

\[ C_{comp} = 20\,\mu F \quad C_{0} = 4\,\mu F \implies C_{c} = 24\,\mu F \]

\[ f_{h} = \frac{1}{\pi \left( \frac{24\,\mu F}{(575.36\,k\Omega) \times (24\,\mu F)} \right)} = 23.05\,kHz \]

LF:

all resistors are within range of \( I_{L} \) = 100\,mA
\[ \frac{1}{40\,\Omega} \approx 0.025 \, \text{mA} \approx 50\,\mu \text{A} \]

\[ C_{c} > \frac{1}{2\pi f_{c} (50\,\mu \text{A})} \approx \frac{1}{318.3}\,\mu F \]

choose \( C = 970\,\mu F \) so \( X_{L} \approx 6.8\,\mu F \)

\[ V_{Ppk} \text{ limit will be due to } V_{Ppk}, \text{ limit is } V_{P} \leq 10\,V_{Ppk} \]

\[ V_{P} = \frac{V_{Ppk}}{\sqrt{2}} \quad R_{E} = 50\,\Omega \quad R_{L} = 8.33\,k\Omega \]

\[ V_{P} = V_{Ppk} \frac{R_{E}}{R_{L} + R_{E} + R_{P}} = V_{Ppk} \frac{0.33\,k\Omega}{8.33\,k\Omega + 7.56\,k\Omega} \]

\[ V_{P} \leq 1.9\,mV_{Ppk} \]

Gain of 7 stage is \(-54.1\) needs to be taken into account.

\[ V_{out} = 1.0279 \cdot V_{Ppk} = 2.06\,V_{Ppk} \]

Supply voltage rail should be taken into account.
Discussion on Hand Design Values

DC Bias conditions

We found that using the spreadsheet definitely decreased the time needed to do one design iteration. It also increased our understanding of the of the material and effects each component had on the rest of the circuit because changes to one part of the circuit were easily propagated to the rest of the circuit.

We followed our design strategy pretty closely using the Darlington stage to guarantee a high input resistance. Then we worried about getting the output swing requirements on the output while ignoring the emitter degeneracy in Q3 to overshoot gain. Because $R_{E2a}$ affects the gain input resistance of the second stage, it has a significant effect on the thevenin equivalent gain of both the first and second stages. At this point, the total amplifier gain was nearly 6000 and the second stage had a higher gain than the first. We slowly increased $R_{E2a}$ while keeping $R_E$ constant until the total gain was brought within the specification and the gain distribution was nearer to our parameter guide.

Next we picked the values of the large bypass and coupling caps to have a near zero resistance at our maximum lower cutoff frequency. From Lab 4 we learned that capacitances around 200 to 500 µF are needed. Using the formula for capacitive reactance, where $X_C = 1/(2\pi fC)$, a 470 µF capacitor has a resistance of 6.8Ω at 50Hz. This is negligible compared to the other resistances in the circuit, so we can be sure that our lower frequency limit is below 50Hz. For the compensation capacitor, we assumed that it caused the dominant pole in the frequency response so we ignored other capacitances. Using the technique developed by comparison with Accusim, we selected a capacitor of 24 pF. When we subtract the estimated $C_\mu$, we get a value of the compensation capacitor of 20 pF.

The last step of hand calculation was to run though and check to see if we had met all the specifications. Although we were able to meet almost all of them, it turned out that we had designed for too high an output resistance. However, with a design that met all the rest of the specifications both by hand and Accusim, we felt that the design was adequate.
ACCUSIM simulation results of DC-Bias conditions (with assumed B=150)
Vout Swing and Rin

Vout = (994.58m + 1.125) = 2.0697Vppk

Rin = Vin/lin = 269.92uV/882.2pA = 305.9kohms

Gain of First stage: Av1 = (2.3496 - 2.3877)/(269.92u + 269.74u) = 70.6
Rout = Vout/\text{Iout} = \frac{9.9215\text{uV}}{232.7\text{nA}} = 42.6\text{ohm}
In lab value measurements (Voltage, Current & Components)

Currents are calculated from $I = V/R$
\[ A_{V_{in}} = \frac{462.5 \text{ mV}}{100.0 \text{ mV}} \cdot 926 = 428.3 \]

\[ V_{in} = \frac{10.6 \text{ V} + 9.81 \text{ V}}{16.6} = 926 \text{ V} \]
HP54645A System A.02.06 21:10:35 Tue Dec 3, 2002

Freq(1)=23.01kHz Vp-p(1)=96.87mV Vp-p(2)=325.0mV

Vertical State Volts/div Position Coupling BW limit Invert Probe
1 on 100.0mV 171.9mV ac off off 10:1
2 on 200.0mV -400.0mV ac off off 10:1

Horizontal Mode Main s/div Delay Reference
main 10.00us 0.000 s center

Trigger Source Level Slope Coupling Rej NoiseRej Holdoff
edge extern 3.492 V + dc off off 200.0ns

Display Mode average: 4
Discussion on Experimental Results

Primary Results

Upon initial power up, we had to wait a very long time for the circuit to reach near its specified DC bias points. This “warm-up” period is to the time constant of the coupling and bypass capacitors, most notably the input coupling capacitor $C_{in}$. The equivalent resistance that $C_{in}$ sees is approximately $R_{b1}/R_{b2} \approx 400k\Omega$. The time constant of an RC circuit is $t=RC=400k\Omega \cdot 470\mu\Omega = 188$ seconds, which corresponds to the capacitor charging to 63% of its steady state value. An RC circuit takes about 5 time constants to reach 99% of its steady state value and this corresponds to approximately 16 minutes. Disconnecting power or the input source resulted in the capacitor discharging. This made measurements in lab someone time consuming.

Once the circuit had reached approximately steady state, the measured amplifier parameters matched very well with both hand calculations and computer simulations. The equation 

$$\%err = 100 \cdot \frac{|LabValue - AccusimValue|}{AccusimValue}$$

is used to evaluate percent error deviation of lab measurements with respect to the simulated values. The only two measurements that were significantly off were mid-band gain and output peak voltage. They were still within specification but higher than simulations by 10% and 25% respectively. All the other parameter measurements were well within 2% of the Accusim simulations. Furthermore, the DC bias measurements were also well matched to simulation. In the second and third stages, all the voltage and current measurements agree within 3% of each other. However, in the first Darlington stage, there is slightly more variation, up to 12%, caused mainly by the current gain multiplication effects of the Darlington pair. It is rather remarkable that the values match this well, especially given that hand calculations and simulations assumed all transistors had uniform current gain and Early voltage. Two factors that helped achieve such good matching were the use of 1% tolerance RC55 series resistors for the biasing network, and a good design that was insensitive to moderate changes in individual transistor parameters.

Failure Modes

Initially, we constructed in the circuit in the Student Projects Lab (SPLab) next door to the EECS 311 lab room due to a lack of available space. At this point the circuit was totally stable in all respects. However, moving the circuit into the EECS 311 lab room generated three distinct results that could be classified as failure modes. These failure modes were sporadic and intermittent. It seemed that the location of people, equipment and wiring in the lab significantly affected when and how the failure modes appeared. The first failure mode was a oscillation of the power supply current draw, which manifested itself in conjunction with the other failure modes. Normally, the circuit would draw 15mA, but in this failure mode the power supply current would ramp down to 0mA and then spike up to 25mA with an oscillation rate between 0.5 and 6 seconds. The circuit would not amplify any signal but would produce output spikes that corresponded with the supply current peaks and dips. In the second failure mode, the circuit would go into ultrasonic oscillation at around 15MHz and again not amplify any input signal. The last failure mode was significant low frequency oscillations with a frequency near 6Hz. Interestingly enough, the only way to prevent these failure modes, which only occurred in the EECS 311 lab, was to hold a voltmeter probe on the positive supply rail beside the last output stage.
HF oscillation in Failure mode.

HP54645A System A 02.06  18:16:26 Wed Dec 4, 2002

Freq(2)=15.15MHz

Vertical | State | Volts/div | Position | Coupling | BW limit | Invert | Probe
1 | on | 700.0mV | 333.8mV | ac | off | off | 1:1 A
2 | on | 200.0mV | -409.2mV | ac | off | off | 10:1 A

Horizontal | Mode | Main s/div | Delay | Reference
main | 100.0ns | 0.000 s | center

Trigger | Source | Level | Slope | Coupling | Rej | NoiseRej | Holdoff
edge | 2 | 0.000 V | + | dc | 1f | on | 200.0ns

Display | Mode | normal

Failure Mode 2.
HF Isolate oscillation.
Failure mode: Low frequency oscillation.

HP54645A System A.02.06  18:33:31 Wed Dec 4, 2002

Vertical State Volts/div Position Coupling BW limit Invert Probe
1 on 200.0mV 393.8mV ac off off 1:1 A
2 on 1.000 V -2.031 V ac off off 10:1 A

Horizontal Mode Main s/div Delay Reference
main 100.0ms 0.000 s center

Trigger Source Level Slope Coupling Rej NoiseRej Holdoff
edge extern 0.000 V + dc 1f on 500.2us

Display Mode normal

Failure mode 3

Low Frequency Oscillation
Summary

Summary of specifications for each stage of design:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
<th>Hand Calculations</th>
<th>ACCUSIM</th>
<th>Lab Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVMID</td>
<td>2625 – 4375</td>
<td>3790</td>
<td>3872</td>
<td>4283</td>
</tr>
<tr>
<td>f_L</td>
<td>&lt;50Hz</td>
<td>&lt;&lt;50Hz</td>
<td>7.72Hz</td>
<td>7.94Hz</td>
</tr>
<tr>
<td>f_H</td>
<td>21kHz – 25kHz</td>
<td>23.05kHz</td>
<td>23.22kHz</td>
<td>23.01kHz</td>
</tr>
<tr>
<td>R_in</td>
<td>&gt;100kO</td>
<td>310kO</td>
<td>305.9kO</td>
<td>N/M</td>
</tr>
<tr>
<td>R_out</td>
<td>&lt;25O</td>
<td>48.45O *</td>
<td>42.6O *</td>
<td>N/M</td>
</tr>
<tr>
<td>V_oppk</td>
<td>&gt;2.0V_ppk</td>
<td>2.06V_ppk</td>
<td>&gt;2.0697V_ppk</td>
<td>2.594V_ppk</td>
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<tr>
<td>I_pwr</td>
<td>&lt;25mA</td>
<td>15.5mA</td>
<td>15.3mA</td>
<td>15.07mA</td>
</tr>
<tr>
<td>R_Load</td>
<td>200O</td>
<td>200O</td>
<td>200O</td>
<td>201.1O</td>
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<tr>
<td>R_s</td>
<td>4.00kO</td>
<td>4.00kO</td>
<td>4.00kO</td>
<td>3.925kO</td>
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<tr>
<td># Transistors</td>
<td>&lt;4</td>
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<td>4</td>
<td>4</td>
</tr>
<tr>
<td># Capacitors</td>
<td>&lt;5</td>
<td>5</td>
<td>5</td>
<td>5</td>
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<tr>
<td>Bias Stability</td>
<td>βR_E&gt;10R_B</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>I_bias&gt;10I_b</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Did not meet specifications

N/M: Was not measured.

Conclusion

Our design met all the specifications except the output impedance. Since we were unable to measure the output impedance of the circuit in the laboratory, we do not know what the exact value of it was, but our hand calculations and ACCUSIM simulation gave a very high value, so we expect it to be higher than the specifications. The only way to decrease the output impedance is to decrease the equivalent resistance of the first two stages, requiring a completely new design. Given the time constraint, we decided not to redo everything.

In all other aspects our circuit performed much better than the given specifications; our output impedance is three times higher than the required minimum, undistorted swing is 60% larger than the required minimum, while power consumption is 37% less than the maximum, voltage gain is within the requirements, high frequency cut-off is right on target and the low frequency cut-off is about one sixth of the required maximum.

As seen on the table above; measured, simulated and calculated values are very close to each other. In fact other than the voltage gain, they are almost identical. The difference between the measured and simulated gains can be due to parasitic capacitances which were ignored or variances in device parameters, as we did not characterize each of the transistors.