BandPass Sigma-Delta Modulator for wideband IF signals

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1.0 Abstract

In this project, a design for a BandPass Sigma-Delta modulator at the IF stage of an RF receiver is presented. Much attention is given to topology choice and circuit non-idealities analysis. A low power solution is achieved using double sampling and multiple path techniques.

2.0 Introduction

Sigma-Delta modulation techniques have been applied to narrow-band passband signals [Jantzi93]. Recent technology improvement has allowed conversion of GSM channels [Ong97] and DECT channels[Bazarjiani97]. In this report, the main concept behind BandPass Sigma-Delta conversion is briefly explained together with its advantages and applications. The architecture choices for this design are then discussed. Finally, the main building blocks and the circuit non-idealities are both analyzed analytically and simulated with appropriate tools.

2.1 BandPass SigmaDelta basics

In BaseBand Sigma-Delta converters, the zeros of the Noise Transfer Function (NTF) are placed close to, or at DC to shape the quantization noise. In a

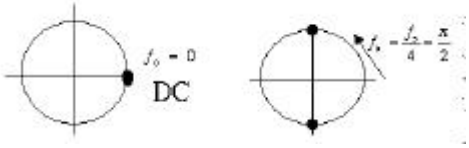

Fig. 1 NTF zeros in Baseband and BandPass converters.

BandPass convert, the zeros of the NTF are moved along the unit circle to the signal center frequency f0 as shown in Fig.1. This is obtained by using a band pass loop filter instead of a low pass loop filter (Fig. 2).

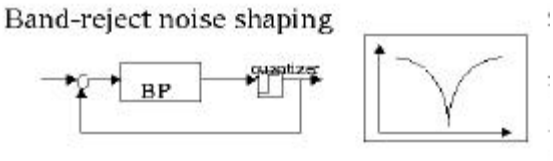

Fig.2 BandPass Sigma Delta converter

2.2 BandPass converter advantages and disadvantages

BandPass converts require double the order of BaseBand converters to obtain the same performance. Also, a wide band sample and hold circuit is required. In turns, BandPass converters:

- maintain the same advantages of BaseBand converters over Nyquist rate converters;
- are insensitive to 1/f noise;
- can provide robust solutions for RF receiver paths as shown in the next section.

2.3 BandPass at the IF stage

When bandpass converters are used at the Intermediate Frequency (IF) stage of RF systems as in Fig.3:

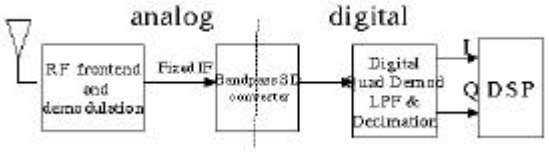

Fig. 3 A/D conversion at IF stage

- analog component count is greatly reduced and testability improved;
- higher flexibility to multiple standard is achieved;
- phase errors and I/Q channel mismatch are avoided by using a very simple and robust digital quadrature demodulation.
- requirements on the preceding image filter remain anyway very difficult for an "on-chip" solution.

3.0 Specifications

Specifications for our design have been derived considering:

- the switching frequency achievable with the targeted 0.35um CMOS technology;
- typical values of IF's in an RF system, and the band requirement of a DECT channel;
- An additional constrain between sampling frequency and center frequency (fs=4*f0) given by the baseband to passband transformation we used in our design.

TABLE 1. Design Specifications

Technology	0.35 CMOS
First IF	189 MHz
Second IF	21 MHz
Sampling frequency	84 MHz
Signal Bandwidth	1.728 MHz
Dynamic Range	56 dB

Fig.4 shows two possible applications for our modulator. Appendix 11.1 discusses briefly some requirements for the filters in front of the converter.

4.0 Architecture

A single loop with one bit DAC architecture can provide enough DR range for our specifications, resulting in the most practical solution for our design. Multibit and miltiloop cascade architectures can probably provide higher DR performance, but they are more difficult to design and less robust to component matching.

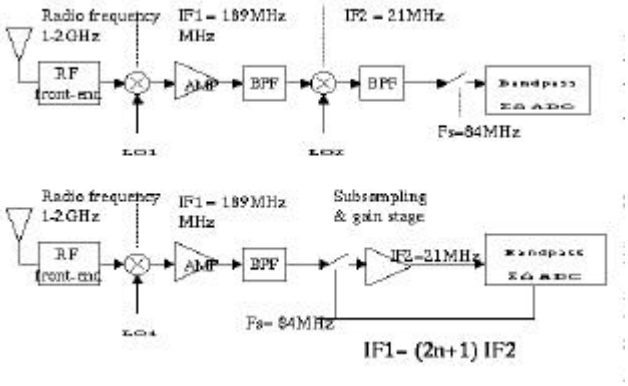

Fig.4 Two applications for our modulator.

4.1 Loop order selection

Several simulations have been performed to select the order of the modulator. For each simulation, NTF zeros have been automatically optimized as shown in Appendix 11.2 using a matlab routine. Fig. 5 shows the SNR curve vs. input signal for 4th, 6th and 8th order bandpass converters. A minimum margin of 12 dB for the quantization noise above the final required DR of 56 dB has been budgeted to account for non-idealities (6dB) and thermal noise (6dB). From our simulations, an 8th order converter gives a DR of 75 dB which satisfies our requirements.

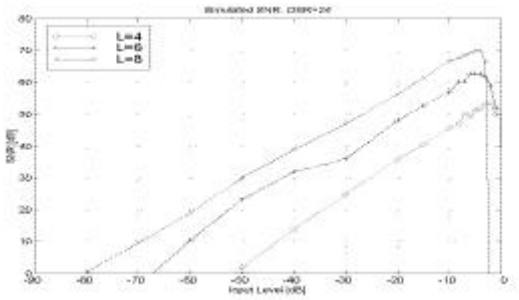

Fig. 5 Simulations to select modulator order. An 8th order gives DR=75 dB which satisfies our requirements.

5.0 Topology selection

5.1 Bandpass design from baseband modulator

A common way to design a bandpass converter is to design a correspondent baseband modulator with the same bandwidth, and then apply a transformation in the z domain. In this design we use the transformation $z \to -z^2$ which moves the center frequency from DC to fs/4. For every pair of complex conjugate zeros of the NTF $z = |\rho| e^{\pm j\alpha}$, we obtain four zeros at

$$z = \sqrt{|\rho|}\, e^{\pm j\left(\frac{\alpha}{2} \pm \frac{\pi}{2}\right)}$$

such that the zeros that before where spread over the baseband [0,B], are now spread over the passband [-B/2,B/2].

5.2 Cascade of resonators with feedback topology

A way to realize the mentioned transformation is realizing the modulator with a cascade of resonators in stead of a cascade of integrators. Fig. 8 shows the topology chosen for our design: a cascade of 4 resonators with feedback coefficients from the digital output.

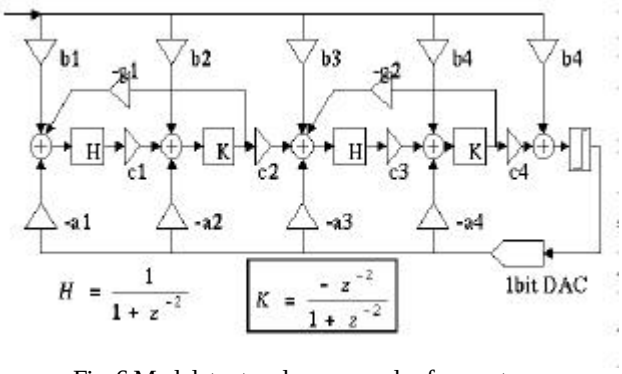

Fig. 6 Modulator topology: cascade of resonators.

Topology coefficients are shown in Table 2. Their spread (i.e capacitor spread) is 98.

TABLE 2. Topology coefficients

a	b	c	g
0.3978	0.3978	0.1128	0.0176
0.3233	0.3233	0.2987	0.0235
0.3716	0.3716	0.5404	
0.3662	0.3662	1.7349	

The 4 resonators are closed in two local feedback loops by coefficients g1 and g2. Such local feedback loops are responsible for the fine positioning of the zeros of the NTF in the passband. This can be easily seen by considering for example the root locus of the system in Fig. 9. The transfer function of the loop is

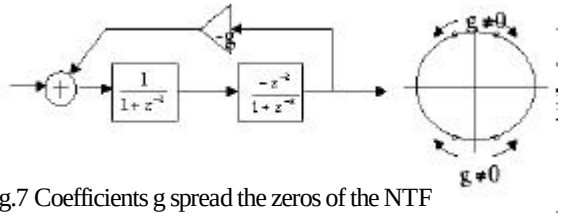

Fig.7 Coefficients g spread the zeros of the NTF along the signal band

$$H_l = \frac{-z^{-2}}{1 + (2-g)z^{-2} + z^{-4}}$$

This structure with a zero delay resonator, as oppose to a loop with two non-zero delay resonators, constrains the zeros of the NTF to be on the unit circle. This is particularly useful when the band is wide as in our design.

The topology has also been slightly modified as shown in Appendix 11.3 to avoid the settling of two amplifiers at the same time. Only "non-zero" delay resonators are used in the final structure. Its functionality has been verified by Simulink simulations. Appendix 11.4 shows the resulting passband noise shaped spectrum.

5.3 Sensitivity to coefficient variations

The chosen topology is very insensitive to coefficient variations. This has been verified by a Montecarlo simulation where the coefficients have been generated random from a gaussian distribution. Only 3dB of DR degradation have been observed with even 10% coefficients variations.

As an alternative to using resonators, the zeros of the NTF could have been placed in passband also by using a loop similar to Fig.9 with integrators inside. In that case the coefficient g realizes both the fine inband zeros optimization and the main transformation from baseband to passband. Anyway, that topology would have been much more sensitive to coefficient variations, because just a 0.1% variation in g would move the NTF zeros of 840kHz missing completely the passband.

5.4 - Stability

When the $z \rightarrow -z^2$ transformation is use, it can be shown that if the correspondent baseband converter is stable, then also the bandpass converter is stable [Norsworthy97]. The stability of the baseband converter has been tested applying increasing DC levels for a million simulation cycles. The output of each resonators are plotted in Fig. Input levels as high as 50% of the value of the DAC output can be safely applied to the modulator. From the same figure it can be seen how the modulator coefficients have been scaled to normalize the maximum value of each resonator output to half an LSB.

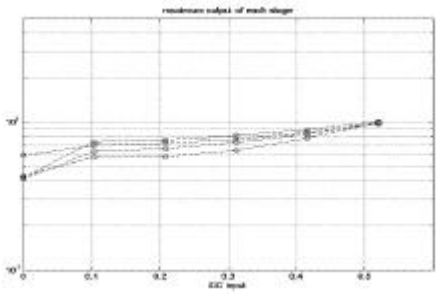

Fig.8 Stability test and scaling: maximum values of each resonator output for different DC inputs on the equivalent baseband converter

6.0 Resonator Implementation

The transfer function of our resonator is realized by the circuit in Fig. 9. One of the main goals for our design was to achieve a low power solution.

6.1 Double sampling

Double sampling has been used to reduce settling time requirements. While the output rate is 84 MHz, the settling time for the amplifier is 12nsec which would normally correspond to an equivalent 42 MHz clock. With double sampling, the sampling capacitor of the next stage is charged together with the integrating capacitor. This anyway is not an issue in our design because the sampling capacitors are usually quite small as they realize small resonator gains. Amplifiers feedback factors are therefore not too smaller then unity.

6.2 Partial Multiple path

We also used a "partial" multiple path structure in which different paths share the same amplifier. Every amplifier realizes two poles and a total of 5 amplifiers have been used to realize an 8th order modulator. This is made possible by exploiting the 2 delay structure of our resonator: "even" samples can be integrated separately from "odd" samples. The feedback factor is not effected by the big number of sampling capacitors shown in Fig. 9 as only two of them (differential) are seen by the amplifier at each phase instant.

The summing nodes in Fig. 6 can be realized by using many sampling structure as in Fig. 9 all connecting to the same amplifier. The feedback factor is affected by such connections, but even for the worst case it is not smaller then 0.2.

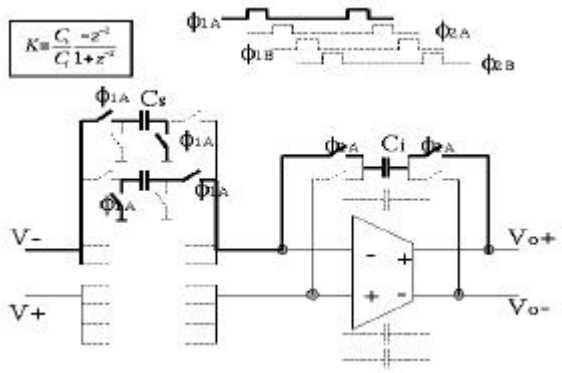

Fig. 9 Double sampled differential resonator.

6.3 Functionality

The functionality of the resonator can be understood considering the desired time domain behavior. As in a non-inverting integrator, at time t, the input that was sampled two phases before, is now transferred to the integrating capacitor which was storing the output of two phases before.

$$C_I y(t) = -[C_I y(t-2) + C_S x(t-2)]$$

Fig. 10 shows a switcap simulation verifying the functionality of the resonator.

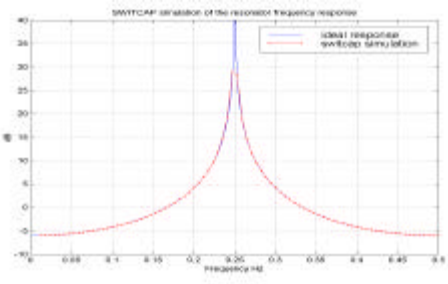

Fig. 10 Switcap resonator simulation compared to matlab.

7.0 Non-idealities analysis

7.1 Finite bandwidth and coefficient variations

Assuming a linear amplifier settling, finite bandwidth changes the topology coefficients of Fig. 8 by a factor $g^1 = \exp\left(-\frac{ts}{\tau}\right)$ which adds to the effect of capacitor mismatch. The overall effect on our resonator transfer function is

$$K(z) = \frac{C_S}{C_I}(1-g)\frac{-z^{-2}}{1+z^{-2}}$$

where g accounts both for finite bandwidth effect g' and for capacitor variations.

7.2 Finite amplifier gain

An analytical formula has been derived in Appendix 11.5 to characterize the effect of finite open loop gain in our resonators. Using these formulas we have included amplifier gain effects in our Simulink simulations. A similar formula has been found in [Ong97] for a simple integrator (there is a typo in that paper: p should read 1-p in one of their formulas).

$$K(z) = \frac{C_s}{C_I}\cdot(1-m)\frac{-z^{-2}}{1+pz^{-2}}$$

$$m = \frac{1}{A}\cdot\left(1+\frac{C_s}{C_I}\right) \qquad p = \frac{1+\frac{1}{A}}{1+\frac{1}{A}\cdot\left(1+\frac{C_s}{C_I}\right)}$$

7.3 Thermal noise

Thermal noise is dominated by the kT/C noise of the first stage. Such noise is reduced by our oversampling ration R=24. Thermal noise is not an issue in our design because of our small DR specification (56dB). From our calculations, capacitor sizing is dominated by mismatch rather then thermal noise: (a minimum of 15fF is required for thermal noise, but we chose a minimum 50fF capacitor). Spread is 98.

7.4 Multiple path mismatch

A "partial" multiple path approach has been used in our implementation.

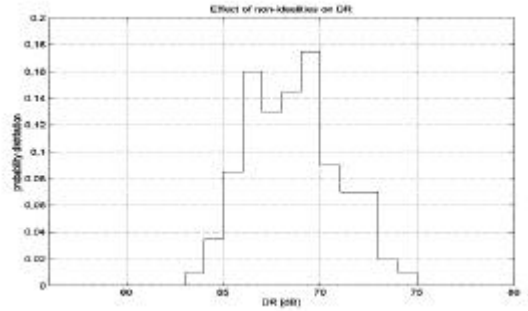

Fig. 11 Monecarlo simulations including finite bandwidth, finite gain and multipath capacitor mismatch.

Capacitor mismatch between paths has been found to degrade DR performance by up to 9-10 dB as shown by the Montecarlo analysis in Fig. 11 and described in Appendix 11.4. For small input signals, in Fig. 12 an image of the signal can also be observed 40dB below itself, which does not represent a main problem for our application. Our multiple paths share the same amplifier, so (besides saving power) amplifier parameters mismatch problems are avoided. Clock mismatch between paths is not an issue when a 84MHz sample and hold is used before the modulator to subsample the first IF and produce the second IF. Such circuit is feasible with a .35 CMOS technology.

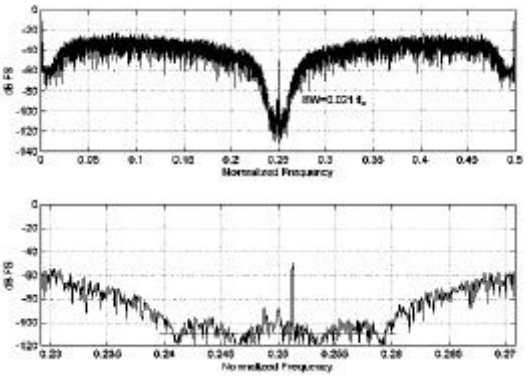

Fig. 12 Spectrum for at -50dB input level including all non-idealities. Note image due to multipath mismatch at -40dB from signal.

8.0 Demodulation and decimation

Quadrature demodulation in our system can be easily performed digitally as shown in Fig. 13 After the demodulation a standard baseband filtering and decimation has been used.

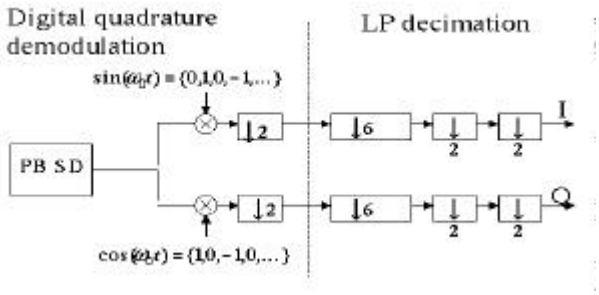

Fig. 13 Digital quadrature demodulation and decimation.

9.0 Conclusions

A design of a BandPass SigmaDelta converter has been developed. BandPass conversion at IF stage is a valuable alternative to baseband systems. In our design we have traded some performance for power using double sampling and partial multiple path. For our application such trade was acceptable and worthwhile, but careful simulation of multipath effects on distortion and DR degradation should be evaluated case by case in other designs.

10.0 Bibliography

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[Shreier97] R. Schreier, " Matlab Sigma-Delta toolbox", ftp:// next242.ece.orst.edu/pub/

[Norsworthy97] S. R. Norsworthy, R. Shreier, G. C. Temes, " Delta-Sigma Data Converters", IEEE Press, 1997.

11.0 APPENDIX

11.1 Filter requirements for the RF systems in Fig 4

If subsampling is used to convert the first IF at 189MHz to the second IF at 21 MHz, a quite selective high pass filter is needed with stop band at 189 MHz -21*2 MHz = 147MHz. This is probably an external precision filter.

If the demodulation to the second IF is obtained using a local oscillator, an antialiasing filter is also needed before the modulator sample and hold. We assume a lot of the channel prefiltering has already been done in the previous stages, in this way not much signal will be present at 3/4 fs = 63MHz the aliasing frequency for our passband at 21MHz. A low pass filter could be used. Specifications for this filter are: passband corner (21+1.728/2) MHz, stopband begins at (3*21-1.728/2)MHz. If this filter is to be realized with RC elements, a 30% component variation in both directions should be taken into account giving the following final specs: passband = 28.8MHz and stopband = 47MHz. This is not a simple filter to realize if a large attenuation is necessary.

In the hypothesis of a good channel prefiltering, a 4th order Chebychev 1 realized with a Fallen and Key structure could be used. Achievable attenuation is only 20 dB. Resistance values can be chosen 20k and capacitors values are Cb1=0.56 pF, Cb2=0.32 pF, Ca1=1.36pF, Ca2=50fF. The two sections have Q's 0.67 and 2.63. If 20dB of attenuation are not enough, a higher order filter should be used. And a ladder topology should be probably chosen to realize such filter.

11.2 NTF zeros optimization

The noise transfer function (NTF) is responsible for minimizing the in-band noise power in a Sigma Delta modulator and it is thus the most important modulator parameter. An optimization approach has been used as shown in [Jantzi94]. Constrains are:

- realizability (NTF(inf)=1)
- stability |NTF(z)|<1.65.

The objective of the optimization procedure is to maximize in-band attenuation. To performed this task a matlab optimization routine has been used [Schreirer97].

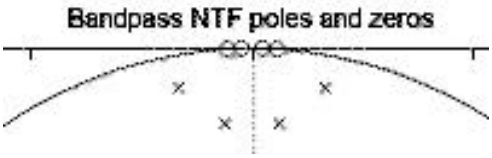

Fig. 14 Optimal position of zeros and poles of NTF.

For example Fig. 14 and 15 show the resulting optimal position for zeros and poles of the NTF and their frequency response for an 8th order modulator.

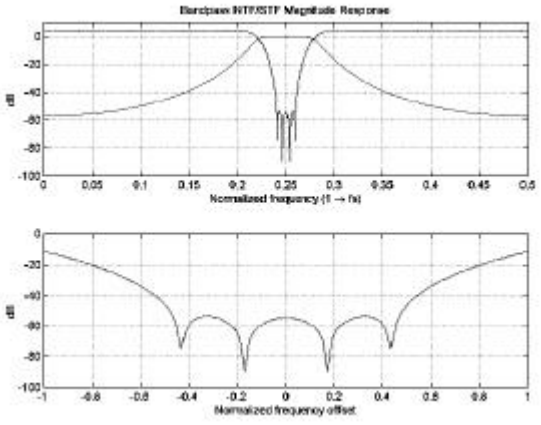

Fig. 15 NTF and STF frequency response.

11.3 How to avoid Zero delay resonators

As shown in Fig. 16, we have used loops with zero delay resonators. To avoid the settling of two amplifiers at the same time, we modified the topology as shown in Fig.16. Such modification does not effect the NTF, but only non-zero delay resonators are needed.

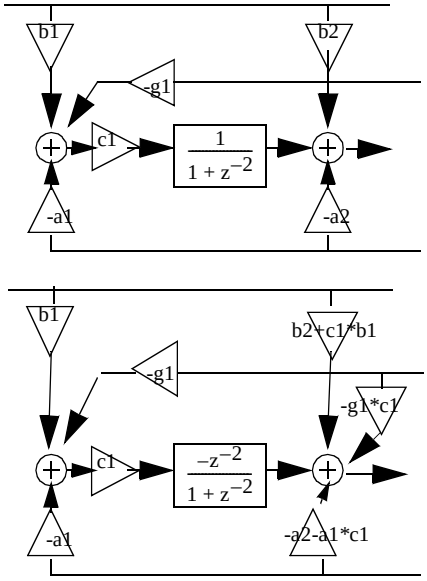

Fig. 16 Zero delay resonators are substituted by non-zero delay resonators.

11.4 Noise shaping simulation

In Fig. 17 we report the bandpass noise shaping spectrum from a Simulink simulation of our modulator.

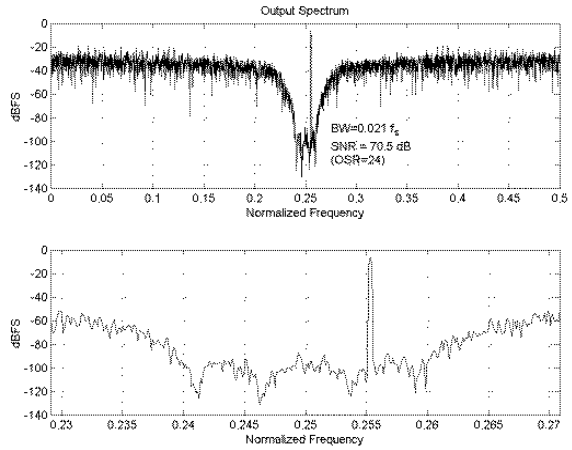

Fig. 17 Noise shaping simulation. Input is -5.5dB.

11.5 Open loop gain effect on resonator transfer function

Considering the resonator in Fig. 9, the effect of finite amplifier gain can be analyzed analytically. At time t, the charge in Ci was

Ci [Vo(t-2) - Vampin(t-2)] , the charge sampled in Cs was Cs Vi(t-2),

but only Cs [Vi(t-2) - Vampin(t)] is transferred to Ci at time t.

Finally the value stored in Ci at the end of the charge transfer is

Ci [Vo(t) - Vampin(t)]. Equating all the previous:

Ci [Vo(t) - Vampin(t)] = - {Ci [Vo(t-2) - Vampin(t-2) + Cs [Vi(t-2) - Vampin(t)] }.

Substituting Vo = -A Vampin and solving, we find the expression reported in Section 7.2. A similar expression has been found also in [Ong97] where eq.(5), (6) and (7) refer to a non-inverting integrator. In that paper eq(7) has probably a typo and its left side p1 should probably read (1-p1).

I derived such equation for a non inverting non differential integrator using:

Ci [Vo(t) - Vampin(t)] = Ci [Vo(t-1) - Vampin(t-1)] + Cs [Vi(t-1) + Vampin(t)],

and I substituted Vo = -A Vampin.

11.6 Simulation of Multipath mismatch

Multipath mismatch effects have been carefully analyzed using in our Simulink simulations blocks as in Fig. 18 in place of every resonator. As shown

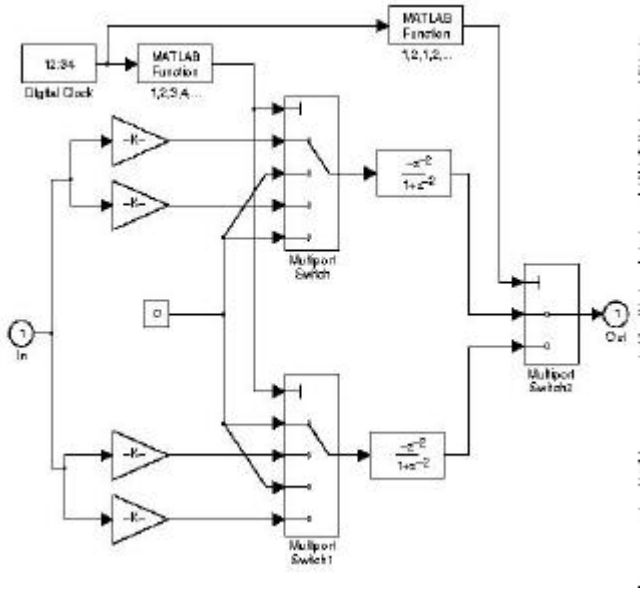

Fig. 18 Block used in place of every resonator of Fig. 6 to model multipath mismatch. Even and Odd samples are integrated separately. Random path gains model capacitors mismatch and are generated at the beginning of every simulation.

in Section 6.2, “even” samples are integrated completely independently from “odd” samples. This is modeled in our simulation by the two resonators in Fig. 18. Mismatch between these two resonators does not need to be accounted for because in the actual circuit implementation the two paths share the same amplifier. But both even samples and odd samples are stored alternatively in two different sampling capacitors. The mismatch between these two capacitors is modeled by random path gains with unity average and gaussian distribution mismatch of 0.5% (99.7% of capacitors are generated within -0.5% and +0.5%). Two hundred simulations have been performed. At the beginning of every simulation, path gains inside each resonators are chosen random and the final DR is calculated from the simulation. Fig. 11 shows the results of this analysis. Multipath mismatch

does affect substantially our system performance degrading the DR from a nominal 75 dB to as low as 65dB. But still these values allow us to meet our specifications.