Design of a minimum power, low-voltage supply fully-differential transconductance amplifier for A/D converters

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Abstract– Two designs of a fully differential transconductance amplifier to be used in a first stage of a pipelined 13-Bit A/D converter are developed and presented. A three stage amplifier achieves the lowest power design. The dynamic range specification is met according to the expression for noise power indicated in the design specification sheet. In this report, anyway, we show that such expression is incorrect for a Miller compensated topology. A second design is developed to meet the specifications according to a more accurate expression of the noise power. Much higher power consumption is obtained even from an optimized design. Miller compensation techniques are inferred to be inadequate to address low-noise low-power specifications.

1 Introduction

Pipelined analog to Digital (A/D) converters usually require transconductance amplifiers to provide an adding functionality and a gain stage. In this project we designed a fully-differential amplifier to be used as a first stage of a pipelined 13-Bit A/D converter according to the following specifications:

Supply	$3.3V \pm 10\%$
Open-loop gain	10000
Settling time	100ns
Accuracy	0.01%
Power	minimum
Dynamic Range	80dB

In order to accomplish this purpose, different topologies could be used. Because of the high gain specification a single stage amplifier is not appropriate and we focused on multi-stage amplifiers. We developed two designs: one uses a three-stages topology, while the other is a folded-cascode with a second stage. In the three stages approach we maintained the topology as simple as possible. Cascodes are not needed, which makes it more robust to supply changes. On the other hand compensation appears more problematic then the two stage design.

For our first design we used an expression for the calculation of the dynamic range which is not accurate for Miller-compensated multi-stage amplifiers. In this report we derive a more accurate expression for our multistage amplifiers. We still present in Appendix A our three stages amplifier which is a low power solution, designed to meet the specifications according to the wrong expression of the dynamic range.

Modifications on the two stages approach seemed more feasible based on the time available after deriving the accurate formula for the dynamic range. The two stages folded cascode, in fact, has been redesigned and optimized for low power in order to meet also the dynamic range specification according to the new expression.

2 General design analysis and optimization

In this section results from our analysis on the trade-offs involved in meeting the dynamic range specification and the trade-offs involved in meeting the settling time specification are presented. These consideration are valid both in the case of the three stages and in the case of the two stages amplifiers.

2.1 Dynamic Range

Assuming the noise power density is given by the expression

$$P_{noise} = \frac{KT}{C_s}(1 + n_f), \tag{1}$$

the dynamic range specification of 80 dB corresponds to:

$$\frac{v_i^2}{8}\frac{C_s}{K \cdot T \cdot (1 + n_s)} \geq 10^8, \tag{2}$$

which translates into:

$$v_i^2 \cdot C_s \geq 8.28 \cdot \mathrm{V}^2\mathrm{pF}, \tag{3}$$

where a noise factor $n_f = 1.5$ has been assumed. A small single-ended input range v_i requires a large capacitor C_s and therefore a large current to drive it.

$$v_i = 0.1 \rightarrow C_s \geq 828\mathrm{pF}$$

$$v_i = 1 \rightarrow C_s \geq 8.28\mathrm{pF}$$

Due to the square dependence on v_i, to minimize power we minimize C_s making v_i as large as possible. This is done avoiding cascodes on the last stage and using small V_d^{sat}.

The noise factor n_f should also be minimized for low power. Small V_d^{sat} in the input transistors and large V_d^{sat} in their loads are used to accomplish the task. We also designed a high gain in the first stage to minimize any additional noise from the later stages.

The expression given above for the noise power density is a good approximation in the case, for example, of a single stage amplifier, where the bandwidth is given by the load capacitor C_s. In a Miller compensated multi-stage approach, the bandwidth is instead given by the compensation capacitor C_c. We show in Appendix B the derivations of a more accurate expression to estimate the noise power for that case:

$$P_{noise} = \frac{KT}{2C_s} + \frac{2n_f KT}{3f_{FB}C_c}, \tag{4}$$

where f_{FB} is the feedback factor that we calculate including also the input capacitance C_{in} of the amplifier:

$$f_{FB} = \frac{\frac{C_s}{2}}{\frac{C_s}{2} + C_{in}}. \tag{5}$$

If the wrong formula is used when designing a Miller compensated multi-stage amplifier, the compensation capacitors are chosen as small as possible to minimize the power. Smaller compensation capacitors require smaller currents for a given slew rate and smaller transconductances which means again smaller currents for a given bandwidth.

If instead the correct formula is used, the compensation capacitor cannot be made small. C_c has to be chosen of at least the same order of magnitude of C_s implying larger power dissipation. An optimal ratio C_c/C_s with respect to power consumption has been found in the case of the two stage folded cascode and the details of the design are presented in Section 3.

2.2 Settling time

The specification on the settling time t_{ST} determines the unity gain bandwidth ω_u. In our designs the slew rate (SR) is given by the tail current in the first stage I_0 and by the capacitor determining the bandwidth:

- the compensation capacitor C_c for the two stages topology,
- the outer-most compensation capacitor C_{c2} in the three stages topology.

The differential output slew rate is

$$SR = 2\frac{I_0}{C_{c2}}. \tag{6}$$

According to the calculations presented in Appendix C the total settling time is:

$$t_{ST} = \frac{2}{\omega_u}[(\frac{2v_i}{V_{gs} - V_t} - \frac{1}{f_{FB}})] - \frac{1}{f_{FB} \cdot \omega_u} ln(\xi \frac{2fv_i}{V_{gs} - V_t}) \tag{7}$$

where ξ is the specified accuracy; $f_{FB} = 1/3$ is the feedback factor. Finally $V_{gs} - V_t$ is the maximum input that does not cause slewing. This quantity can be chosen to trade slewing time with linear settling time. We observed that in our design, for low power a minimum value of $V_{gs} - V_t$ is to be chosen to minimize the noise factor n_f and to achieve high transconductance in the first stage with smaller current.

The unity gain bandwidth is chosen as low as needed to meet the settling time specification. In our design we chose the following parameters:

3 Two-stage approach

In this section a two stages folded cascode amplifier design as in Fig. 1 is presented. The amplifier has been

Design	$V_{gs} - V_t$	v_i	f_u
three stages	150 mV	1.0V	69 MHz
two stages	120 mV	1.23V	91 MHz

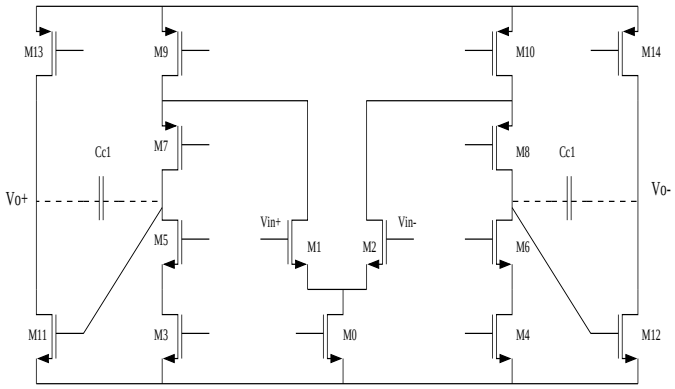

Figure 1: Two stages folded cascode schematic

designed specifically to meet the specification on the dynamic range using the expression for the noise power derived in appendix B. The design has been optimized in order to minimize the power consumption which results anyway considerably large with respect to the three stages approach. Part of the reason for that is the fact the noise strongly depends also on the compensation capacitor C_c which then needs to be made large leading to large power.

In addition to the general design considerations already presented in section 2 and valid for both the three stages and the two stages topology we have introduced optimizations specific for the topology used in this design.

3.1 Noise factor optimizations

The gain from the first stage, a folded cascode, is very high. The input referred noise will then be mostly dominated by the input devices M1-M2 and their noisy loads in the folded cascode M3-M4 and M9-M10. The noise factor in this case is:

$$n_f = 1 + 2\frac{V_{d1,2}^{sat}}{V_{d9,10}^{sat}} + \frac{V_{d1,2}^{sat}}{V_{d3,4}^{sat}}. \tag{8}$$

In order to minimize n_f:

- we chose a small $V_{d1,2}^{sat} = 120$ mV for the input devices. This is also good to achieve a large transconductance with lower current;
- we chose the V_d^{sat} of the loads M3-M4 and M9-M10 as large as possible by minimizing the V_d^{sat} of the cascodes M5-M6 and M7-M8. We have checked that the third pole given by the cascode devices M7-M8 is still at very high frequency $f_{3rd} = 1.6$GHz not affecting the phase margin;
- the devices M9-M10 carry double the current of M3-M4 so we chose $V_{d9,10}^{sat}$ larger then $V_{d3,4}^{sat}$;
- we also used larger lengths in the loads to reduce the flicker noise factor $L_3 = L_4 = L_9 = L_{10} = 1.8\mu$m.

3.2 Noise power optimization

As shown in appendix B, the noise power for a Miller compensated amplifier used in a gain stage of a A/D pipelined converter is:

$$\bar{v}_{in}^2 = \frac{KT}{2C_s} + \frac{KT}{C_c}\frac{2n_f}{3f_{FB}} \tag{9}$$

$$= \frac{KT}{C_s}\left(\frac{1}{2} + \frac{2n_f}{3f_{FB}\frac{C_c}{C_s}}\right). \tag{10}$$

Assuming a noise factor $n_f = 1.58$ and an input step $v_i = 1.23$V from the optimization for minimum current shown in appendix D we found that the best value for the ratio C_c/C_s is 2.17 and we chose $C_c = 10pF$, $C_s = 4.6pF$ in order to meet the dynamic range specifications.

3.3 Design parameters

In Table 1 are summarized the main design parameters.

Table 1: Parameters of two stages design. Refer to Fig. 1

	size [μm]	V_d^{sat}[mV]	$I_{bias}[\mu$A]	g_m[mS]
M1-M2	342/0.6	120 mV	444	6.6
M3-M4	120/1.8	322 mV	444	
M5-M6	510/0.6	100 mV	444	
M7-M8	510/0.6	165 mV	444	
M9-M10	85.2/1.8	1100 mV	888	
M11-M12	684/0.6	132 mV	1132	14.3
M13-M14	684/0.6	215 mV	1132	

The current and the transconductances are very large due to the large value of capacitors needed to meet the dynamic range specification. Some of the devices are approaching velocity saturation so the current has to be even larger to attain the desired g_m. Also the devices have very large sizes. We included their gate capacitances in our optimization routines hence HSPICE simulations confirmed our calculations. The overall design seems not to be very practical anyway from an area and power point of view.

3.4 Bias network

The bias network is one of the most crucial parts in a design of a folded cascode. Supply variations and process variations can make the bias points move if ratio design and supply independent current bias are not used. In Fig 2 a significant part of our bias network is shown.

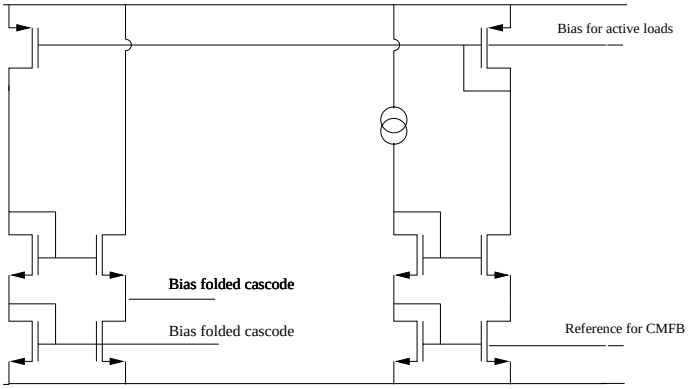

Figure 2: Part of the bias network

- The cascode devices are biased in order to use all the available supply range in the worst case.
- We mirror the reference currents using supply independent schemes.
- For matching purposes we chose to use relatively large reference currents (100μA) for the mirror MOSFETs biasing the devices carrying large currents (1mA). For this reason also the bias network is using a lot of power.

3.5 Common Mode FeedBack

We used a dynamic switch capacitor common mode feedback (CMFB). In a two stage amplifier, if a single CMFB is to be used, the output common mode needs to be inverted before being applied for example to the tail current or a load of the first stage. We solved this problem applying the feedback not directly to the load but to the transistor producing the reference current to be mirrored in the load as shown in Fig. 3, thus obtaining the inversion . To avoid common mode ringing in the step response we reduced the g_m of that transistor by increasing its V_d^{sat}.

3.6 Results

A summary showing the overall performance with respect to the assigned specifications in the nominal and worst conditions is presented in Table 2.

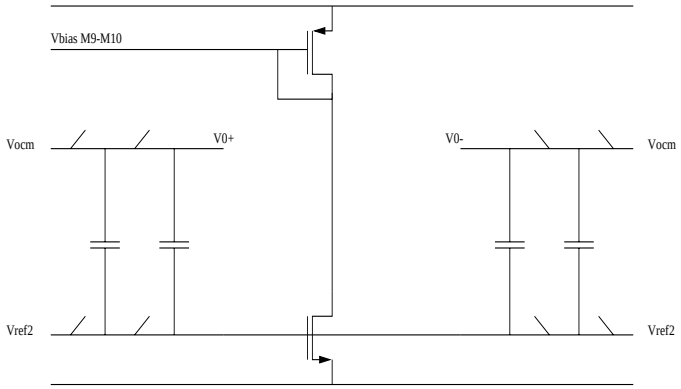

Figure 3: CMFB network

Table 2: Performance summary table of the two stage design.

	$V_{dd} = 3.0$ slow	$V_{dd} = 3.3$ nom	$V_{dd} = 3.6$ fast
DR	80.14 dB	80.14 dB	80.14 dB
A_{vo}	32170	15000	8800
t_{slew}	56 ns	48 ns	36 ns
t_{tot}	90 ns	80 ns	70 ns

The specification on the gain is not met in the case of higher supply voltage combined with a fast process. We used supply independent current bias but we could not limit gain variations which seem to be determined mostly by the process variation. For the same bias voltages a fast process implies higher currents that increase with a square root relationship the transconductances but decreases linearly the output resistances overall decreasing the gain. Reducing the current on the second stage is a way to overcome this problem, but in this way we decrease the zero and second pole frequencies decreasing the phase margin and producing some overshooting and oscillations in the step response. Decreasing the current on the first stage, instead helps increasing its gain and improves phase margin. Bandwidth and speed is usually not a problem with the fast case but can become a problem with the slow process.

3.7 Power analysis

Even though every effort has been done to minimize the power, the choice of this topology did not allow us to achieve a low power solution when the right expression for the noise power in appendix B is used. Table 3 shows a breakdown of the power in our circuit. The first stage is using almost as much power as the second stage be-

Table 3: Power breakdown for the two stages design.

	$V_{dd} = 3.0$ slow	$V_{dd} = 3.3$ nominal	$V_{dd} = 3.6$ fast
1st stage	4.2 mW	5.9 mW	7.2 mW
2nd stage	5.4 mW	7.5 mW	10.5 mW
bias network	1.3 mW	1.8 mW	2.1 mW
total	10.9 mW	15.2 mW	19.8 mW

cause it is driving a very large compensation capacitor, and because the folded cascode requires a current 1.5 times larger than a regular telescopic stage. We remind that the compensation capacitor has to be chosen so large because it determines the power noise according to our calculations.

Also the bias network is using a relatively large power. We deliberately chose not to use small reference currents that would give matching problems when mirrored on large devices to set large currents.

3.8 Frequency and step response

We show in Fig. 4 to Fig. 6 the frequency response of the amplifier. As argued in appendix D we measure the

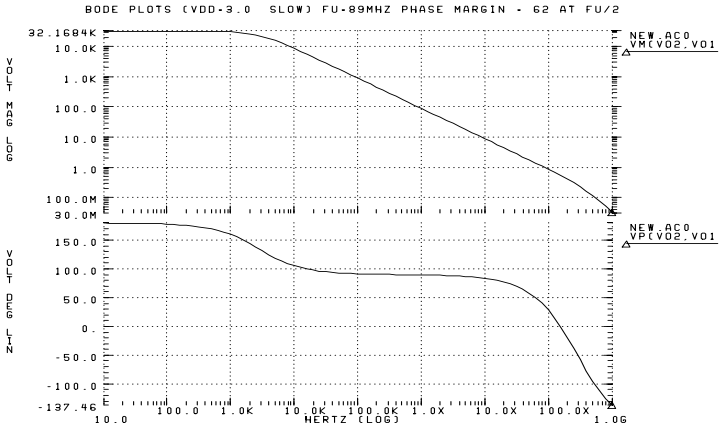

Figure 4: Frequency response for V_dd=3.0 V combined with a slow process.

phase margin at $\omega_u/2$ because this amplifier is specifically designed for a gain of two configuration. From the plots we can see an increasing of the unity gain frequency when a faster process is used. That is probably due to the increasing of the currents.

In Fig. 7 to Fig. 9 are shown the step responses of the amplifier in the capacitive feedback configuration for the A/D converter. The slewing and setting times

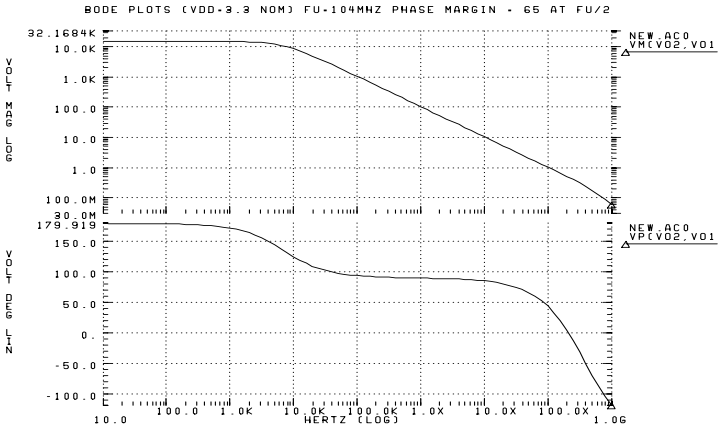

Figure 5: Frequency response for V_dd=3.3 V combined with a nominal process.

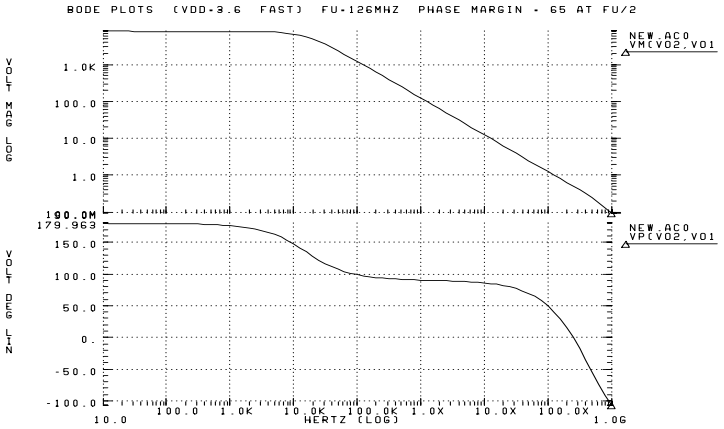

Figure 6: Frequency response for V_dd=3.6 V combined with a fast process.

matches the values calculated using the expressions in appendix C.

3.9 Noise simulations

In Fig. 10 is shown the total power density referred to the input sampling capacitor C_s. In the same figure are also shown its main component: the noise from one of the input devices M1 and the noise from its loads M3 and M9 (refer to Fig. 1). The flicker noise has been set to zero in the simulation by setting to zero the factor K_F. The noise from any other device has been observed to be negligible as expected. The noise factor from our simulations is

$$n_f = 1.55 \qquad (11)$$

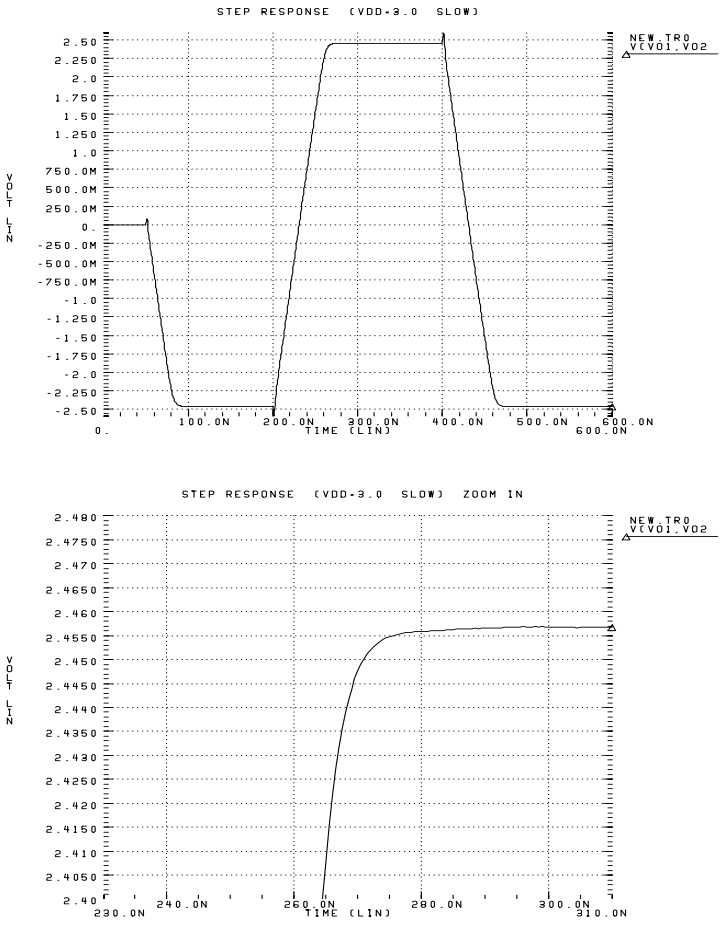

Figure 7: Step response for V_{dd}=3.0 V combined with a slow process.

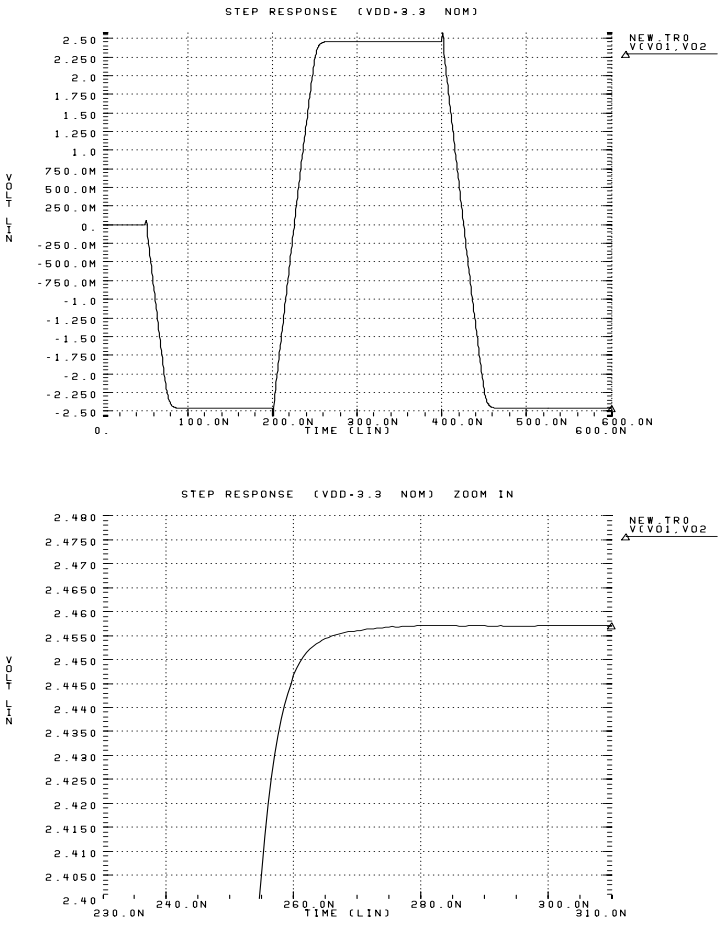

Figure 8: Step response for V_{dd}=3.3 V combined with a nominal process.

which matches the value calculated in our hand analysis within 3%. The noise power referred to the input is

$$P_{noise} = \frac{KT}{2C_s} + \frac{2n_f KT}{3f_{FB}C_c} = 1.83 \cdot 10^{-9} \qquad (12)$$

where the feedback factor including the input capacitance C_{gs1} = .4pF, is f_{FB} = 1/3.17. The total output range for each side is 2.46 V which allows to use an input step v_i = 1.23 V. The dynamic range is 80.14 dB.

3.10 Summary of the two stage design

This design has been realized with the specific intent of meeting also the dynamic range specification using the expression in appendix B. All the devices parameters have been optimized to achieve a minimum power solution for this topology. The purpose of satisfying the dynamic range specification has been achieved. The design meets all the specifications also in the worst cases with the exception of a gain 12% lower then specified in the case of a fast process. The frequency response in the nominal case shows a bandwidth of 104 MHz with a phase margin of 65 degrees in the given close loop configuration and the step response shows a very large differential output range of 4.92 V. The overall power consumption is considerably high ranging from 11mW to 20mW. This is mainly due to the fact that this topology, as any other Miller compensated topology, needs to drive a compensation capacitor in addition to the load capacitor, both very large because of the dynamic range specification.

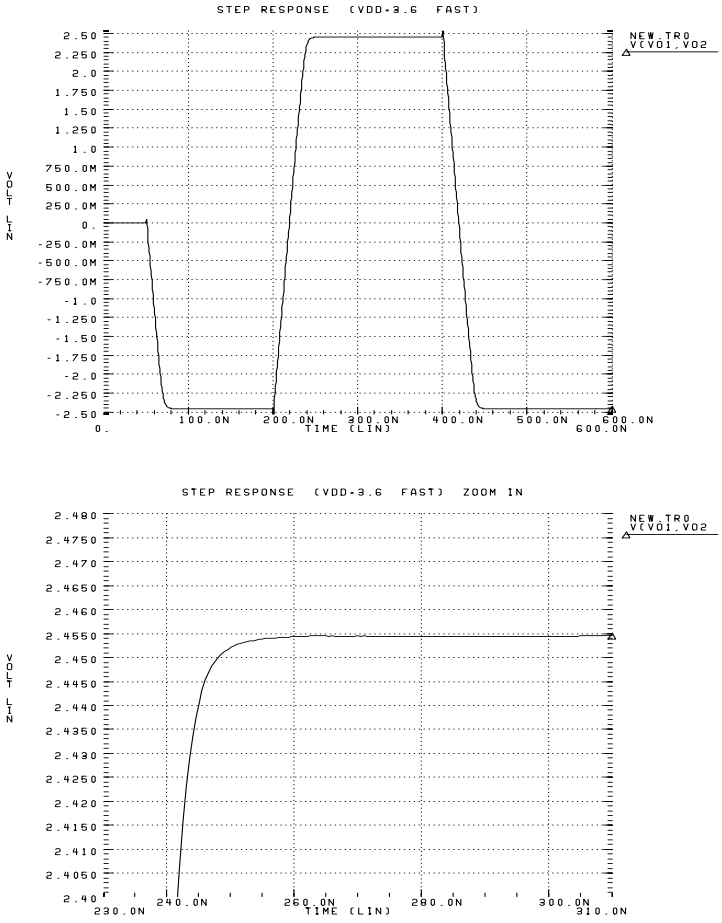

Figure 9: Step response for V_{dd}=3.6 V combined with a fast process.

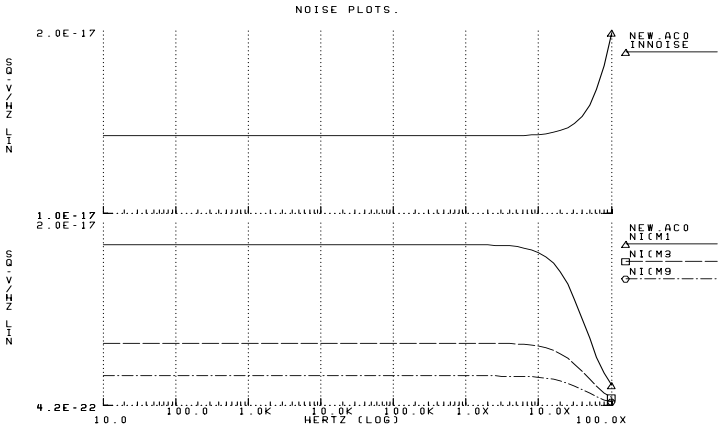

Figure 10: Total input thermal noise power density (linear scale on y-axis) and its breakdown into noise from the input devices M1 and its noisy loads M3 and M9 (logarithmic scale on y-axis.

4 Conclusions

4.1 Consideration on topology choice for low power designs

A three stage design has been presented. That design meets all the specifications when calculated using the given expressions for their estimation. The circuit has power consumption as low as 5 mW. A more accurate expression has then been derived for the dynamic range. The three stage amplifier does not meet that specification according to the new expression.

A two stage folded cascode design was originally developed to compare performance with the three stages one. A three stage amplifier presents a priori a simpler bias network; it is more robust to supply and process variation; finally it has smaller noise factor provided the gain of the first stage is large enough. On the other hand a three stages approach requires difficult nested Miller compensations. Moreover the two stages folded cascode was going to have only slightly higher if not similar power consumption.

After the more accurate expression for the dynamic range has been derived, all the parameters of the two stages design have been modified. The new optimization minimized power consumption satisfying at the same time the dynamic range specification evaluated using the new formula. Simulations confirmed we achieved our purpose. Comparisons a posteriori, yet, on power consumption between the three stage and the two stages are now not possible anymore. The much larger value needed for the compensation capacitance increased its power consumption four to five times. General conclusions about Miller compensated amplifiers can anyway be inferred.

We argue that the same increase would have occurred if also the three stage amplifier was completely redesign to meet the dynamic range specification calculated in the new way. This approximately extends to any multi-stage Miller compensated amplifier where the bandwidth over which the noise is to be integrated is determined by the compensation capacitor C_c. The dynamic range specification would require both a large load capacitor and a large additional capacitor C_c. This leads us to conclude that in general Miller compensated multi-stage amplifiers probably are not the lowest power solution for a high resolution A/D converters.

We suggest that a low-noise low-power amplifier

should be instead designed such that its bandwidth is determined only by the load capacitor C_s. In this way we avoid having to drive the large additional internal compensating capacitor C_c. As a single stage amplifier can hardly provide the specified high gain, at least a two stages approach should be used. The second pole would then be determined by C_{gs2} and C_{gd2} of the second stage together with the output resistance r_{o1} of the first stage. As C_{gs2}, C_{gd2} would not be negligible anyway, the r_{o1} would have to be considerably small. Possible problems with this topology are then a small gain in the first stage; the gain has then to be boosted in the second stage while keeping the output range as large as possible; finally noise from the second stage also becomes an issue. The solution of these problems, though, would probably lead to a much lower power design then ours.

APPENDIX

A Three-stage approach

The use of three stages as the configuration for the amplifier has several advantages as well as some problems. The "a priori" **advantages** are:

- High gain with a simple structure, which does not require cascodes;
- More robust to supply changes;
- and easy to operate with low supply;

The **disadvantages** are:

- Difficult compensation: a nested Miller compensation network is needed;
- May have larger offset and noise contribution;
- A single common mode feedback circuit (CMFB) might not be enough;

These tradeoffs will be verified in the design. The schematic of the design is presented in Fig. 11.

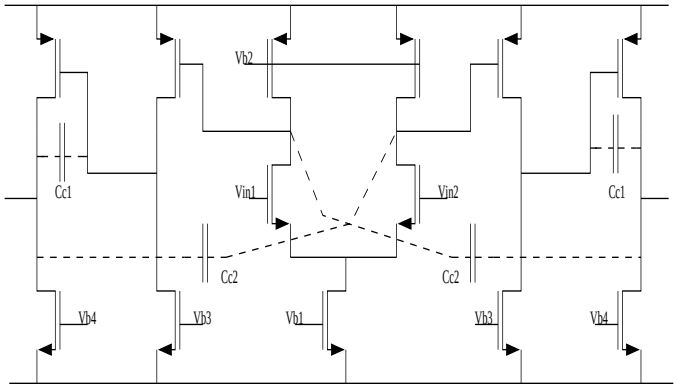

Figure 11: Three stage schematic

The input range $v_i = 1.0V$ and the load capacitor $C_s = 8.28$pF have been chosen according to the dynamic range specification and the incorrect formula (1) in Section 2.1 for the noise power which does not include the compensation capacitor C_c. The specified gain has been split among the three stages in the following way:
First stage —— gain of 50
Second stage —— gain of 30
Third stage —— gain of 10

A high gain has been chosen for the first stage in order to reduce offset and noise contributions from the other stages. Since Miller compensation reduces the bandwidth by a factor of two for each compensation capacitor, a high bandwidth is initially needed.

A.1 Dimensioning the transistors

The first stage has a gain 50 and its initial bandwidth has to be at least $280MHz$ to acquire the $69MHz$ with the compensation capacitors, then:

$$\frac{g_m}{C_L} \geq 280 \cdot 2\pi \cdot 10^6 \tag{13}$$

For C_L we can use a value of $60fF$ because it will drive the gate of a second stage (without the compensation capacitor). This yields $g_m \geq 50\mu S$ and a current of $5\mu A$. This value has been checked in Fig.12 to be out of the weak inversion region. The $V_{D\,sat}$ have to be so that they don't shrink the output swing. We choose

$$V_{dsat2} = 0.15$$

$$V_{dsat4} = 0.3$$

$$V_{dsat1} = 0.3$$

and finally, from

$$I = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{dsat}^2 \tag{14}$$

the ratios needed for the transistors are found. These initial values where adjusted with Spice simulations. To minimize the flicker noise, the input devices could have a larger length, but as this amplifier has to go in an A/D converter, there are techniques to eliminate the flicker noise, so it is not one of our main concerns.

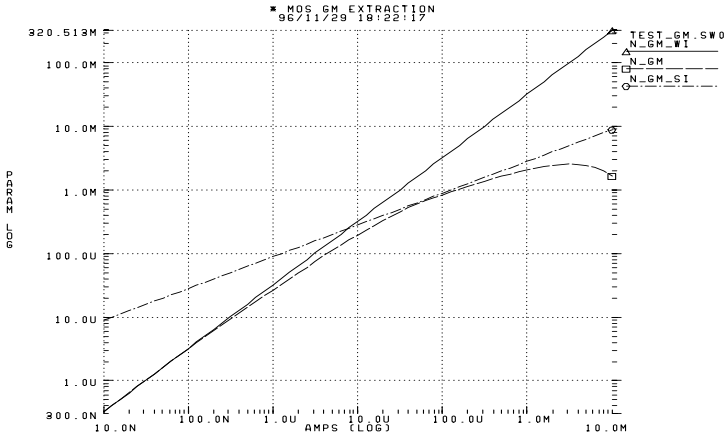

Figure 12: Weak inversion checking

The bias voltages are:

$$V_{B2} = 2.25V$$

$$V_{B1} = 1V$$

The second and third stages are designed in a similar way, but with increasing currents in order not to be limited by slew rate. Specifically, the third stage, has to drive the output capacitor, which is $8.28pF$. Then the currents are:

$$I_{2ndstg} = 40\mu A$$

$$I_{3rdstg} = 650\mu A$$

Finally, the final sizes and reported characteristic parameters are summarized in the following table:

Also there's a need for a CMFB network. There have to be at least 2 networks, for at each output stage the same phenomenon may happen. That is: if the output of one stage goes too high or too low, it may bring the next stage out of saturation and then all the bias voltages would be wrong, causing the amplifier to malfunction

Transistor	Current	Size	Transc.	Vdsat
M1 (N)	10.01u	8/2	84.4u	190 mV
M2,M3 (N)	5.01u	4/1	61.1u	150 mV
M4,M5 (P)	5.01u	4/1	34.0u	242 mV
M21 (P)	46.0u	10/2	116.4u	623 mV
M22 (N)	46.0u	10/2	203.9u	328.9mV
M31 (P)	645.0u	590/1	4.71m	226 mV
M33 (N)	645.0u	240/2	5.7m	173mV

A.2 Bias Network

The bias voltages are drawn from the reference current source of $10\mu A$ that is available, following the structure of Fig.13, and as it appears in [1]. The output lines serve as reference to force the current to go through a saturated device, which is scaled to give the appropriate voltage level.

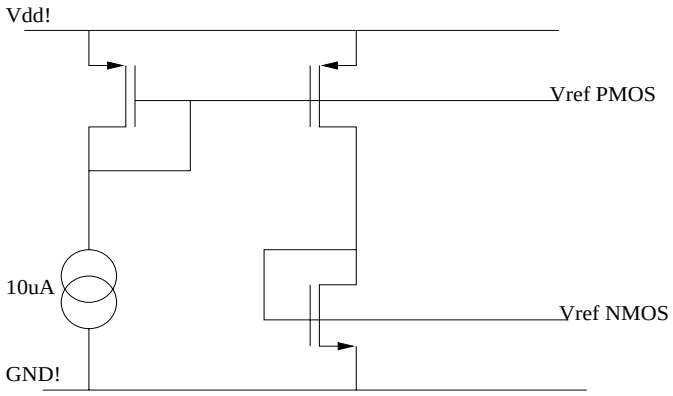

Figure 13: Bias Structure

A.3 Stability and compensation

Using the sizes specified and the accurate bias needed, the frequency and phase responses are, according to HSPICE simulations, as shown in Fig. 14. Obviously, it is unstable, due to the three poles accumulated in the three stages.

Using the simplified model for small signals shown in Fig.15, we derived the expressions for the three poles. The analysis of the poles for the small signal model consist on the application of Kirchoff's laws to the different nodes. We have:

$$v_0 = g_{m6} \cdot v_A \cdot r_{o6} // r_{o7} // \frac{1}{C_L s} \tag{15}$$

$$v_A = g_{m4} \cdot v_B \cdot r_{o5} // r_{o4} // \frac{1}{C_{g4} s} \tag{16}$$

and for the calculation of v_B we use the diagram shown in Fig 15:

$$v_i = \frac{I_1}{C_{g1} s} + I_3 \cdot r_{o3} \tag{17}$$

$$I_3 \cdot r_{o3} = g_{m1} \cdot r_{o1} \cdot (v_i - I_3 \cdot r_{o3}) + I_2 \cdot (r_{o1} + r_{o2} // \frac{1}{C_{g2} s}) \tag{18}$$

$$I_3 \cdot r_{o3} \cdot (1 + g_{m1} \cdot r_{o1}) + I_3 \cdot (r_{o1} + r_{o2} // \frac{1}{C_{g2} s}) = g_{m1} \cdot r_{o1}\, v_i + I_1 \cdot Z_2 \tag{19}$$

$$I_3 = \frac{g_{m1} \cdot r_{o1} + Z_2 \cdot C_{g1} s}{(1 + g_{m1} \cdot r_{o1}) \cdot r_{o3} + Z_2 \cdot (1 + C_{g1} s \cdot r_{o3})} \cdot v_i \tag{20}$$

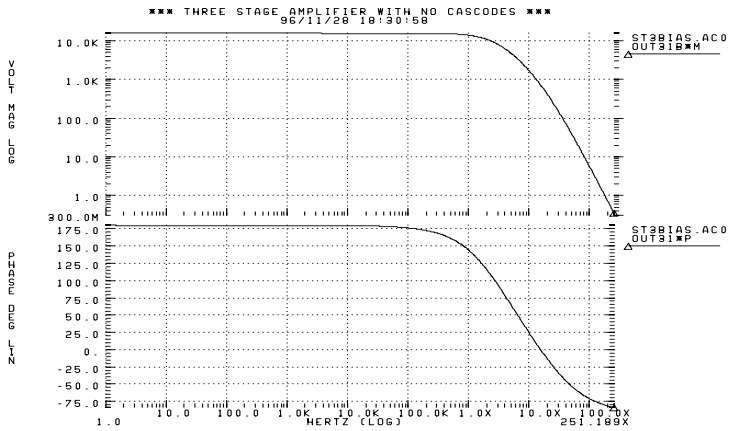

Figure 14: Frequency response

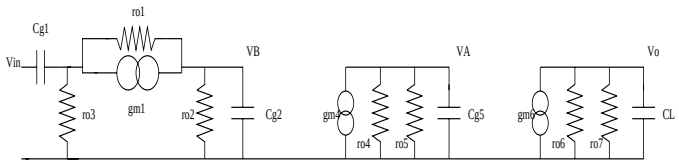

Figure 15: Small Signal Model

$$v_B = \frac{r_{o2}}{1 + r_{o2} C_{g2} s} \cdot \frac{C_{g1} s \cdot r_{o3} - g_{m1} \cdot r_{o1}}{(1 + g_{m1} \cdot r_{o1}) \cdot r_{o3} + Z_2 \cdot (1 + C_{g1} s \cdot r_{o3})} \tag{21}$$

Finally, substituting we can get the desired frequencies of the poles. Notice that there is also one zero, but its frequency is higher than the band of interest. The poles have the following values: $5.7MHz, 12MHz, 20MHz$. The 3 poles are too close together and cause a $60dB/dec$ slope of the frequency response. Therefore, some compensation is needed. The nested Miller Compensation, as described in [1] is used. Because of the inverting nature of each stage the outermost capacitor needs an additional inverting stage. Since the design is fully differential, this additional inversion can be achieved by simply crossing the connections. The pole-splitting can be seen in the Root Locus, calculated with Matlab and shown in Fig. 16

The structure was analyzed and a model used in SPICE to corroborate the expressions of the new poles. These are:

$$P_{dominant} = \frac{1}{r_{op} A_2 A_3 C_{c2}} \tag{22}$$

$$P_{nondominant} = \frac{1}{r_{op2} A_3 C_{c1}} \tag{23}$$

Considering that the bandwidth is $6.9MHz$ the first pole has to be at $6.1KHz$. Also, the second pole has to be at 4 or 3 times the unity gain bandwidth to get a phase margin of 70 degrees. These calculations yield:

$$C_{c2} = 0.127pF, C_{c1} = 55fF$$

These new paths will give zeros, but they are far from the band of interest, placed at $10.12GHz$ and $131GHz$. Therefore, we don't need resistors to null them or to push them further away.

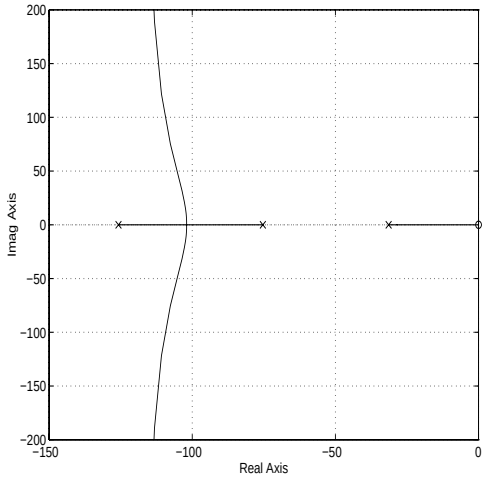

Figure 16: Root Locus

A.4 Common Mode FeedBack circuits

Three CMFB circuits are needed. While it is true that the common modes of the three stages are linked together, for a 10% of uncertainty in the supply voltage, it is much more secure to have the three structures. With only two of them, most specifications can be met, but a third makes the structure more robust to supply variances. Also, this would mean more power consumption.

The structure used is the dynamic one described in class. That is, the one shown in Fig. 17, with the capacitors carefully chosen so as not to interfere with the rest of the network.

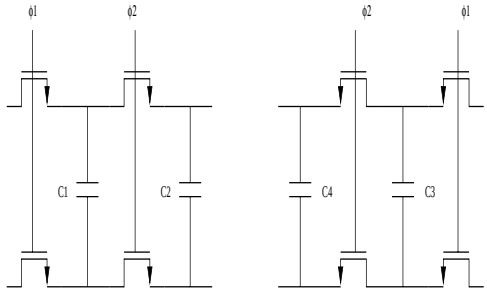

Figure 17: Common Mode Feedback Circuit

A.5 Noise

The noise analysis for this three stages design refers to the formula for the noise power given in the handout. A more accurate formula is derived in appendix B and the two stages design has been modified to meet the dynamic range specification with the new formula.

Performing a noise analysis with HSPICE we observed that most of the noise contribution is flicker noise. Anyway, this is a slow varying noise that can be reduced using different techniques such as two cascaded amplifiers coupled by capacitors that store and subtract the flicker noise as well as the offset. Thus, the flicker noise is not an issue in our design and we set to zero the flicker noise coefficient K_F in the SPICE technology file.

We have estimated the thermal noise with a HSPICE simulation grounding the inputs and integrating in the sampling capacitor C_s the noise. The power density of this noise from hand analysis is

$$\bar{v}_{in}^2 = 4KT\frac{2}{3}g_m^{-1}n_f = 4 \cdot 10^{-16} = \mathrm{V}^2/\mathrm{Hz} \qquad (24)$$

while HSPICE reports a level of $4.5 \cdot 10^{-16}$.

The calculated corner frequency in the case of flicker noise is $f_c = 2.3MHz$, and from SPICE we measured $f_c = 3MHz$. To illustrate the noise and indirectly calculate it, we show in Fig. 18 the reported curves for the thermal noise at the input of the differential pair and at the active loads.

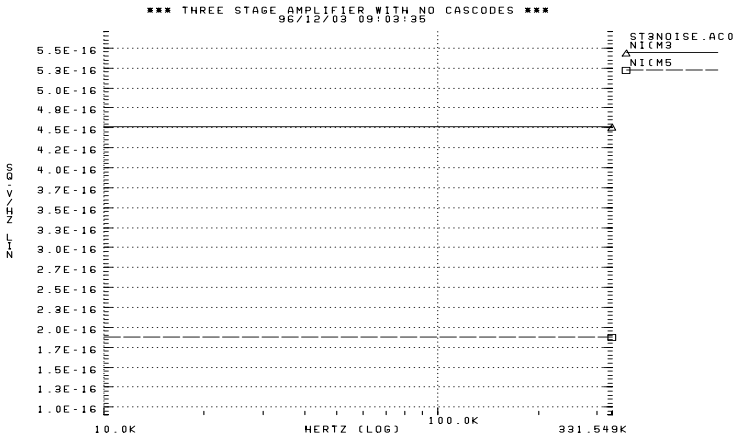

Figure 18: Comparison of both thermal noises: due to the input differential pair (solid line) and the active load (dashed)

The total noise power density including flicker noise is shown in Fig. 19. The total noise power density excluding flicker noise is shown in Fig 20.

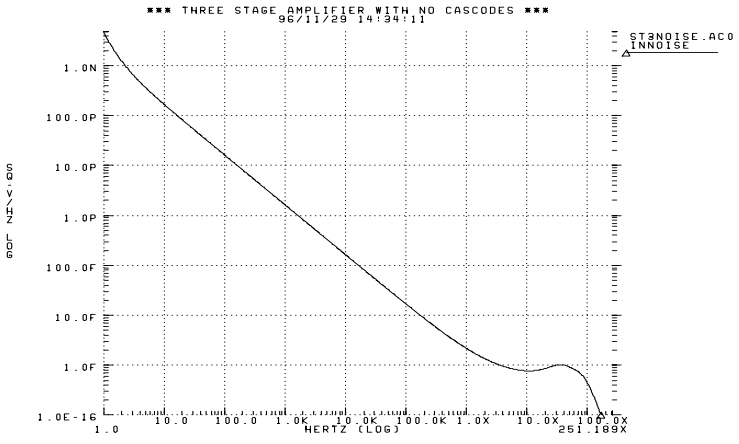

Figure 19: Total noise power density (including flicker noise) referred at the input.

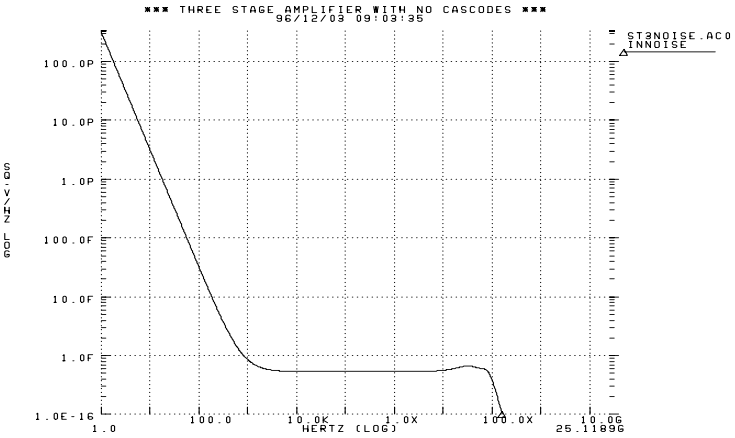

Figure 20: Total noise, excluding flicker noise, referred at the input.

	Current (total)	Power
First Stage	$10\mu A$	$33\mu W$
Second Stage	$100\mu A$	$330\mu W$
Third Stage	$1290\mu A$	$4.26mW$
Bias	$60\mu A$	$198\mu W$

From our measurements we calculated a thermal noise factor of

$$n_f = 1.42$$

Using this value and the formula given in the handout this design has a Dynamic range of 80.12 dB which meets the specifications.

A.6 Power

One of main requirements in this project is the minimization of power consumption. This is an aspect specially adapted to the three stages design. Only that stage driving a big capacitor has to provide a high current. In this case, in the original design, with the incorrect expression of the noise power, the last stage is the one which has to give up to $645\mu A$ and so, it will be the one to consume more power. The overall power reported by SPICE is:

$$Power = 4.818mW$$

we can split this power consumption into the different parts: It should also be mentioned that the .AC statement, where we calculated the power consumption does not consider the CMFB circuits, for they are treated as controlled voltage sources.

A.7 Results

All the designs have been included and simulated with HSPICE. Here we present the results of such simulations. First in Fig. 21, we present the frequency and phase response of the compensated three stages, with a supply voltage of 3.3V. In Fig. 22 and Fig. 23 we present the response to the step. The 1V input step is first applied at 100ns, so the differential output has to be 2V at 200ns, then at 300ns we apply the 2V differential input. Now at 400ns, the differential output has to have swung 4V. This way, the circuit

can swing the full-range. To better appreciate the settling time, the zoom at around 400ns is shown in Fig. 24.

We have measured the settling times of both behaviors: slewing and exponential and they closely match the expression, yielding times of:

$$t_{SR} = 42ns$$

$$t_{exp} = 55ns$$

Also, the response including the dynamic CMFB circuits is shown in Fig. 25. Since it is not as clean as with the controlled voltage sources, we thought that it was clearer to show these responses.

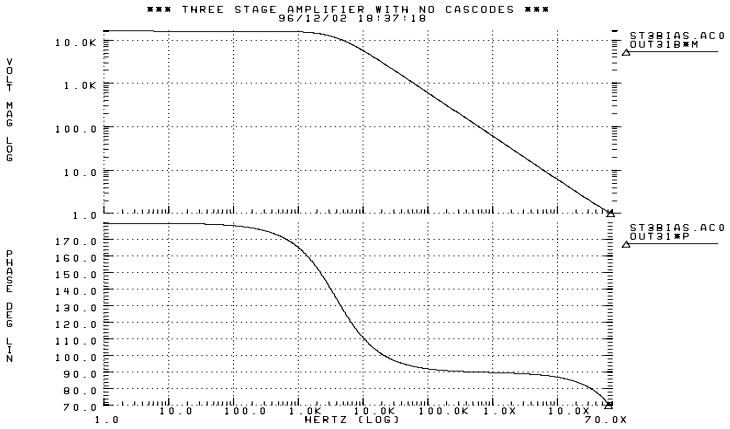

Figure 21: Ac response with a 3.3V supply

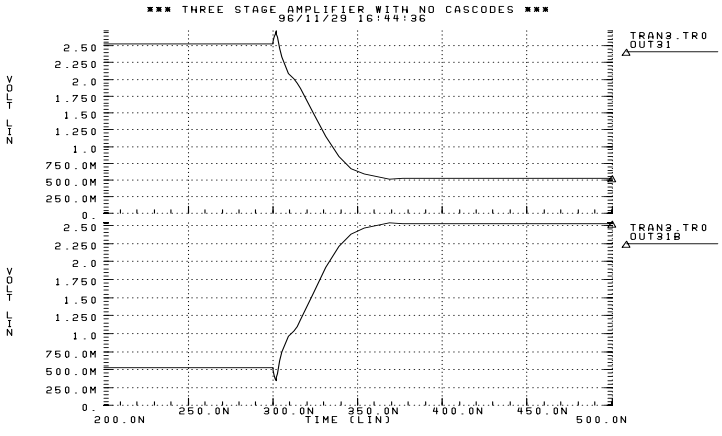

Figure 22: Separated responses of both outputs with the step input

Also, we have to consider the variation in the supply. We have performed the .AC measurement with $V_{dd} = 3.0V$ and $V_{dd} = 3.6V$. The results are shown in Fig. 26 and Fig. 27.

A.8 Modifications to the design

There is an error in the expression used for the dynamic range. For a multi-stage amplifier with compensation capacitor C_c we estimate the noise power as derived in appendix B. The three stage design does not meet the dynamic range specification when calculated according to that expression. We sketch here possible modifications to improve this design. Performance can be improved easily by just increasing the outer most compensation capacitor C_{c2} to 4.1pF and decreasing the load capacitor C_s to 5.38pF. In this way we increase the dynamic range to 76 dB. As we found from our previous design, a Slew Rate of $70\frac{V}{\mu s}$ and a bandwidth of 69MHz are enough to achieve the settling time specifications. Recalculated parameters for the first and third stages using the new modified values for C_{c2} and C_s are shown below:

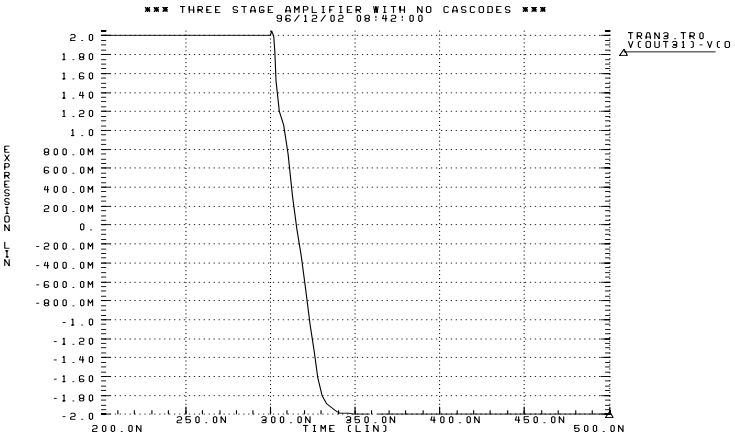

Figure 23: Differential output at the step input

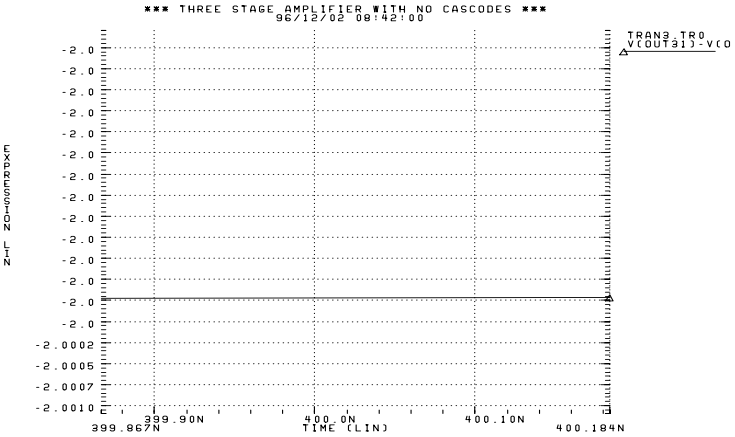

Figure 24: Zoom view of the settling

$$g_{m1} = 1.567mS$$

$$I_{ss} = 282\mu A$$

$$I_3 = 380\mu A$$

$$V_{dsat2} = 179mV$$

$$V_{dsat4} = 360mV$$

$$\frac{W}{L_{nmos}} = 88$$

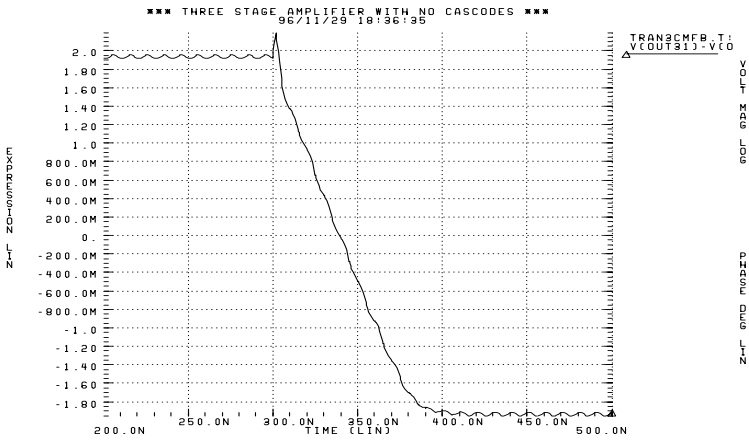

Figure 25: Settling response with the CMFB circuits included

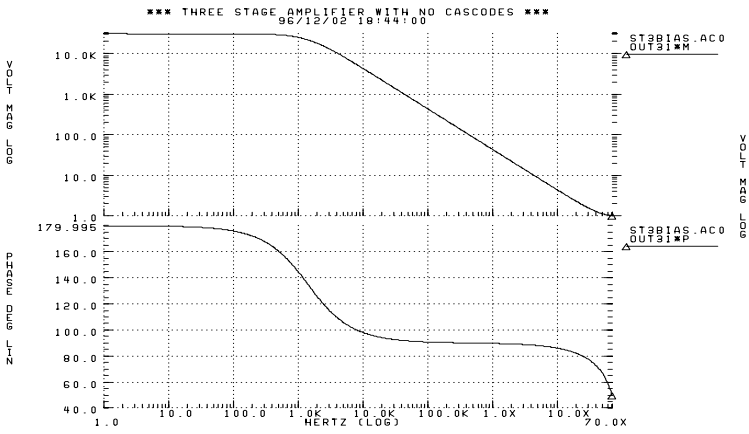

Figure 26: AC response with a 3.0V supply

$$\frac{W}{L_{pmos}} = 48$$

and the response that we observe is the shown in Fig. 28 while if we try to compensate it, we observe the curves in Fig. 29 but still there's a very poor phase margin. Notice that we have not changed the conditions for the second stage which could improve the response. Also we have to mention that the power has gone up to $6.229mW$. This result confirms that the multistage solution can be a low power solution.

A.9 Summary of the Three-stage approach

The design here presented meets the specifications and has a power consumption of about 5mW. In this design we used for the noise power the formula given in the handout which is not accurate for this topology. According to that expression our design has a dynamic range larger then 80 dB but not according to the more accurate expression. Given the time left when we realized that, we could just sketch some modifications of the design improving the

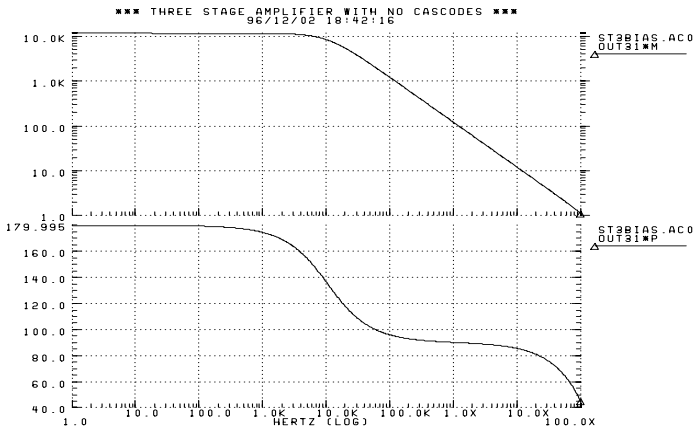

Figure 27: AC response with a 3.6V supply

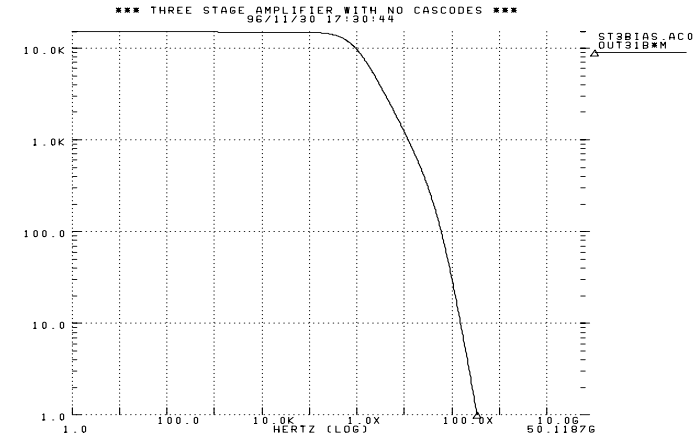

Figure 28: Uncompensated AC response with correct values

actual dynamic range to 76 dB and managing to keep the power low.

B Noise analysis for a multi-stage Miller compensated OTA

In this section a derivation is presented for the noise power of a multi-stage Miller compensated amplifier used in an analog to digital converter.

During the first phase the signal and the noise from the previous stage are store in the input capacitor C_s. That noise is the noise of the amplifier referred to its input

$$\frac{\bar{v}_{eq}^2}{\Delta f} = 4KT\frac{2}{3g_m}n_f, \tag{25}$$

where g_m is the transconductance of the first stage and n_f is the noise factor of the amplifier. The bandwidth and so the noise

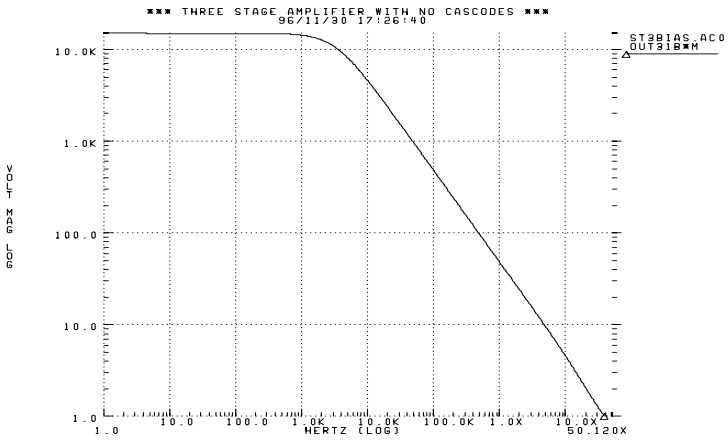

Figure 29: Compensated AC response with correct values

bandwidth of a multi-stage Miller compensated amplifier is generally determined by the outermost compensation capacitor C_c. Applying a feedback configuration with a factor f_{FB} and integrating the noise density over the noise bandwidth the noise in the output is

$$S_t = \frac{KT}{C_c}\frac{2n_f}{3f_{FB}}. \tag{26}$$

During the same sampling phase noise is stored in the feedback capacitor $C_s/2$

$$\bar{v}_{nc}^2 = \frac{KT}{C_s/2}. \tag{27}$$

In the next phase the noise sampled during the first phase in C_s are also transfered to the feedback capacitor producing a total noise in the output

$$\bar{v}_{on}^2 = \frac{KT}{Cs/2} + A_{cl}^2\frac{KT}{C_c}\frac{2n_f}{3f_{FB}}. \tag{28}$$

This noise can be referred to the input dividing by the square of the closed loop gain $A_{cl} = 2$.

$$\bar{v}_{in}^2 = \frac{KT}{A_{cl}^2 C_s/2} + \frac{KT}{C_c}\frac{2n_f}{3f_{FB}} \tag{29}$$

$$= \frac{KT}{2C_s} + \frac{KT}{C_c}\frac{2n_f}{3f_{FB}} \tag{30}$$

We also observed that if large devices are used in the first stage the input capacitance C_{in} of the amplifier can affect the feedback factor:

$$f_{FB} = \frac{\frac{C_s}{2}}{\frac{C_s}{2} + (C_s + C_{in})}. \tag{31}$$

First, we consider that the flicker noise doesn't have to be analyzed because we have seen that there are different ways to eliminate this slow varying time noise, such like two cascaded amplifiers coupled by capacitors that store the flicker noise as well as the offset. Thus, the flicker noise is not much of an issue.

C Settling time computation

The calculation of the settling time has to be splitted into two parts: the slewing and the exponential rising. The first is due to the limitation of current charging a capacitor and the second is due to the response of a one-pole system to a step input. Then, the Slew Rate yields a time of:

$$t_{SR} = \frac{V_{stepo} - V_{mxo}}{SR} \tag{32}$$

where V_{stepo} is the step at the output and V_{mxo} is the maximum output without slewing, both of them single-ended. These values are referred to the input through the feedback factor. Also, we have that

$$SR = \frac{I_0}{C_c}$$

and

$$w_u = \frac{g_m}{C_c}$$

and the maximum input without slewing is

$$V_{mxi} = V_{GS} - V_t$$

then

$$t_{SR} = \frac{2}{w_u}\cdot\left(\frac{2\cdot V_{step}}{V_{GS} - V_t} - \frac{1}{f}\right) \tag{33}$$

the factor of 2 is for this particular case, for it is the gain of the amplifier. As for the settling time when in between the exponential response limits:

$$t_{exp} = \frac{1}{w_{3dB}}\cdot ln\left(\xi\cdot\frac{2\cdot f\cdot V_{step}}{V_{GS} - V_t}\right) \tag{34}$$

Therefore, the total settling time is the sum of both:

$$t_{ST} = \frac{2}{w_u}\cdot\left[\frac{2\cdot V_{step}}{V_{GS} - V_t} - \frac{1}{f}\right] - \frac{1}{f\cdot w_u}\cdot ln\left(\xi\cdot 2\cdot f\cdot\frac{V_{step}}{V_{GS} - V_t}\right) \tag{35}$$

D Two stages capacitor sizing

In this section we outline some parts of the procedure we used to size the compensation capacitor C_c and the load capacitor C_s in order to

- meet the specification on the dynamic range using the formula derived in appendix B;
- meet the specification on the settling time by achieving a 91MHz unity gain bandwidth with 70 degrees of phase margin
- minimize the current.

Referring to the expression for the noise power in appendix B, as a first order optimization we chose to make the contribution to the noise from C_c as large as the one from C_s by choosing $C_c/C_s = 3$. This assumes a noise factor $n_f = 1.5$ and a feedback factor $f_{FB} = 1/3$. For a more careful analysis chose two parameters C_c/C_s and the ratio between the transconductances of the second and first stage g_m1/g_m2. We developed a MATLAB program that optimizes these two ratios for minimum power.

We calculate the phase margin with the expression

$$\phi_m = 90 - \left[tg^{-1}\left(\frac{\omega_u/2}{p_2}\right) + tg^{-1}\left(\frac{\omega_u/2}{z_{ero}}\right) + tg^{-1}\left(\frac{\omega_u/2}{p_3}\right)\right]$$

The amplifier is to be used in a feedback configuration with an overall closed loop gain of two so we calculate the phase margin with respect to the -3 dB frequency $\omega_u/2 = 2\pi 45MHz$, and we

impose the constrain $\phi_m \geq 70$. The second pole p_2 as a function of our two ratio parameters is given by

$$p_2 = \frac{g_m 2}{g_m 1} \frac{C_c}{C_s} \omega_u. \tag{36}$$

The zero is given by

$$z_{ero} = \frac{g_m 2}{g_m 1} \omega_u. \tag{37}$$

References

[1] Eschauzier, R.G.H.; Hogervorst, R.; Huijsing, J.H., "A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6 MHz UGF." IEEE Journal of Solid-State Circuits, Dec. 1994, vol.29, (no.12):1497-504.