Demonstration of 40-Gb/s Packet Routing Using All-Optical Header Processing

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***Abstract*—We show simultaneous forwarding of two optical packets through a 2×2 spatial switch at 40 Gb/s using only two ultrafast nonlinear interferometers. This demonstrates a scalable all-optical header processing architecture applicable for general network topologies and can lead to reduced size, weight, and power requirements as compared with electronic solutions. Clear open eye diagrams were observed and a packet error rate of 10^{-6}, comparable with current electronic router error rates, was measured for the entire system.**

***Index Terms*—Optical fiber communication, ultrafast optical switching.**

I. Introduction

As DEMAND for bandwidth in telecommunication networks grows, both transmission capacity and packet routing node capacity must increase. Transmission capacity can be increased by adding to the number of wavelength channels through techniques such as dense wavelength-division multiplexing and by increasing channel data rates to 40 Gb/s and above. At each routing node, the packet header must be processed and a forwarding decision must be made before the packet can be transmitted to the correct destination. High-capacity packet processing at routing nodes in the network is then necessary to decrease packet processing delay, which reduces the required queue sizes and, thus, congestion in the network.

Electronic processing of high bit rate optical headers currently requires demultiplexing the header to lower data rates followed by optical–electronic–optical (O/E/O) conversions. As network channel data rates increase to 40 Gb/s and beyond, optical signal processing techniques offer several advantages over electronic solutions such as decreased packet processing delay [1], short buffer lengths, transparency to payload bit rate and modulation format [2], [3], power consumption which remains constant with increasing channel data rates, fewer O/E/O conversions, and a more straightforward switch structure requiring fewer input–output ports for the same bandwidth capacity. Optical label swapping techniques can further add to these advantages by reducing the necessary processing in the core of the network. This can lead to reduced size, weight, and power requirements as compared with electronic solutions.

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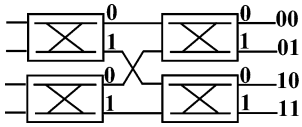

Fig. 1. Example of 4×4 Banyan switch matrix. The first and second bits of the destination address are sufficient to forward packets through the first and second columns of the switch matrix, respectively.

Previous all-optical header processing demonstrations have focused on keyword address recognition for broadcast-and-select networks [4]–[8]. More general network topologies require header processing and forwarding of multiple packets arriving simultaneously. Here, we demonstrate 40-Gb/s all-optical header processing for independent packets simultaneously propagating through both input ports of a 2×2 spatial switch using only two ultrafast optical logic gates. For the ultrafast packet routing architecture described previously by our group [9], this header processing approach also provides unlimited packet address space and scalability of logic density that grows as $N\log N$ with port count N.

II. System Description

In a Banyan switch matrix, only the jth address bit is needed to forward packets through the jth column in the switch matrix (Fig. 1). For this architecture, header processing for two packets simultaneously propagating through a single 2×2 spatial switching element requires only a single address bit for each packet. Furthermore, we define an "Empty/Full" bit, which indicates the absence or presence of data in the packet payload. The "Empty/Full" bit reduces the number of optical logic gates required for accurate forwarding decisions by identifying cases in which the state of the spatial switch does not matter. For instance, when both packets are "Empty," any forwarding decision is acceptable. This control bit can either be included in the packet header or generated in the network node by detecting the average power in a packet. If the "Empty/Full" bit is included in the packet header, a single optical logic gate can be used to demultiplex the "Empty/Full" and address bits onto two separate wavelengths [10].

To achieve the required header processor operation, we use the Boolean logic function $R = E_1 \cdot A_1 + E_2 \cdot \bar{A}_2$, where R indicates the state of the 2×2 switch ("0" = bar, "1" = cross) and E_i and A_i are the "Empty/Full" bit and the address bit, respectively, for the packet on input Port i. If an arriving packet is "Empty" $(E_i = 0)$, the corresponding address is ignored. When both arriving packets are "Empty," the 2×2 switch remains in the bar state. If a "Full" $(E_i = 1)$ packet arrives, the state of the 2×2 spatial switch is set by the address of the

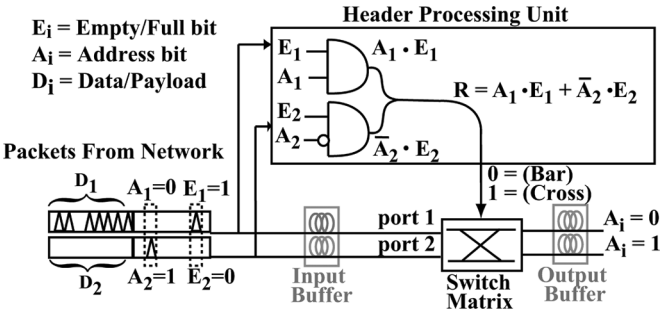

Fig. 2. Single 2×2 unit cell for ultrafast packet routing. Solid lines indicate functions implemented in this demonstration. A_i, E_i, and D_i refer to the address bit, "Empty/Full" bit, and payload, respectively, of the packets arriving on the ith port of the 2×2 electrooptic switch. An address of 0 and 1 direct the packet to the top and bottom output port, respectively, of the 2×2 switch.

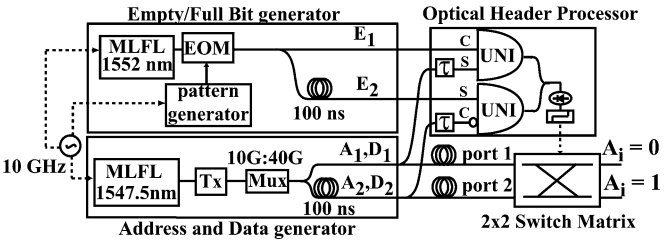

Fig. 3. Experimental implementation of all-optical header processing demonstration. MLFL is a mode-locked fiber laser, Tx is the transmitter, and EOM is the electrooptic modulator. At the UNI inputs, C indicates the control while S indicates the signal. τ shows a fixed delay determining the relevant address bit for this 2×2 electrooptic switch. Finally, A_i, E_i, and D_i are the address bit, "Empty/Full" bit, and payload of the packet arriving at the ith port of the 2×2 switch matrix.

packet if it arrives on Port 1 or by the inverse of the address if it arrives on Port 2. Packets arriving on different input ports of the 2×2 spatial switch require opposite switch states to be forwarded to the same output address. If both packets are "Full," the packet requesting a cross state is prioritized. It is assumed that contention resolution will be implemented elsewhere in the system, either through deflection routing or the implementation of input–output buffering. Input buffers will also be required for synchronization of the two incoming optical packets before progressing through the 2×2 switch matrix. Such buffering will require additional logic which is beyond the scope of this experiment. The ultrafast header processing unit for a single 2×2 spatial switch is shown in Fig. 2.

Fig. 3 shows the experimental setup for the 40-Gb/s packet generator, "Empty/Full" bit generator, header processor, and 2×2 spatial switch. The packet generator creates the address and payload by using a mode-locked fiber laser to produce 2-ps pulses at 1547.5 nm modulated at 10 Gb/s with a $2^7 - 1$ pseudorandom bit sequence (PRBS) and optically multiplexed to 40 Gb/s. By using a $2^7 - 1$ PRBS to generate the packet address, we demonstrate that no address-pattern-dependent effects will preclude the use of this header processing architecture for forwarding packets with 7-bit addresses through a full-scale router with up to 128 input ports. The "Empty/Full" bits are created using a second synchronized mode-locked fiber laser generating 2-ps pulses at 1552 nm modulated with a "1001" repeating pattern at 10 MHz, creating 100-ns packets. Two distinct 2×2 spatial switch inputs are generated by introducing a 100-ns single-packet delay between Ports 1 and 2 packet streams. A similar delay exists between the two "Empty/Full" bits corresponding to the two distinct port inputs. This packet delay allows us to explore all possible combinations of address bits and "Empty/Full" bits for the two packet streams.

To implement the Boolean logic required to make packet forwarding decisions, two ultrafast nonlinear interferometers (UNIs) [11], operating in copropagating mode, are configured as AND gates with coupled outputs providing OR functionality. Through cross-gain and cross-phase modulation in a semiconductor optical amplifier, a UNI gate implements the logical functions of either $S \cdot \bar{C}$ (inverting) or $S \cdot C$ (noninverting), where S is the signal input and C is the control input to the UNI. To generate $E_2 \cdot \bar{A}_2$, we use an inverting UNI gate with the address bit of the packets on Port 2 as the control input and the "Empty/Full" bit as the signal input. For the packets on Port 1, we use a noninverting UNI gate with the "Empty/Full" bit as the control input and the address bit as the signal input. Fixed delay lines on the address bit inputs to the UNI gates determine which address bit the header processing logic operates on. Combining the outputs of the two UNI gates using a passive optical coupler provides the desired Boolean OR logic. Since the control and signal inputs to the noninverting UNI gate are reversed from those of the inverting UNI gate, the two UNI outputs are at different wavelengths and interferometric effects at the combining point are reduced.

The 2×2 spatial switch is implemented using an electrooptic lithium niobate modulator, which provides fast switching times and low crosstalk. To control this switch, the output from the header processor must be converted to an electronic pulse that is temporally matched to the packet duration of 100 ns. To perform this conversion, we use a high-speed 18-GHz photodetector followed by a 10-GHz electronic D-flip-flop. The packet processing delay of the optical header processing block is currently dominated by the 62.5-ns fiber propagation time in the UNI gates. However, monolithically integrated optical logic gates can reduce the total packet processing time to below 1 ns. The switching time of the 2×2 electrooptic spatial switch determines the guard band requirement for the system, and is measured to be approximately 1 ns. This guard band requirement can be reduced to $<$25 ps by implementing the 2×2 electrooptic switch with a travelling-wave electrode using standard modulator designs. The extinction ratio of the 2×2 electrooptic switch is measured to be $>$25 dB, which indicates that low interchannel crosstalk can be achieved between packets transmitted in parallel through both ports.

III. Results

Eye diagrams showing the results of the 40-Gb/s all-optical logic performed by both the noninverting and inverting UNI gates are shown in Fig. 4(a) and (b). Packet error rates of 1.7×10^{-9} and 3×10^{-9}, respectively, were measured for the two UNI gates. The total output of the header processor unit is shown in Fig. 4(c), illustrating the accurate Boolean OR logic of the passive coupler with a packet error rate of 1×10^{-6}, comparable with current electronic router packet error rates. This indicates the low-error packet-forwarding decisions that can be achieved with this all-optical header processing design. The switching energies required for the inverting and noninverting optical logic gates are 33 and 27.5 fJ, respectively.

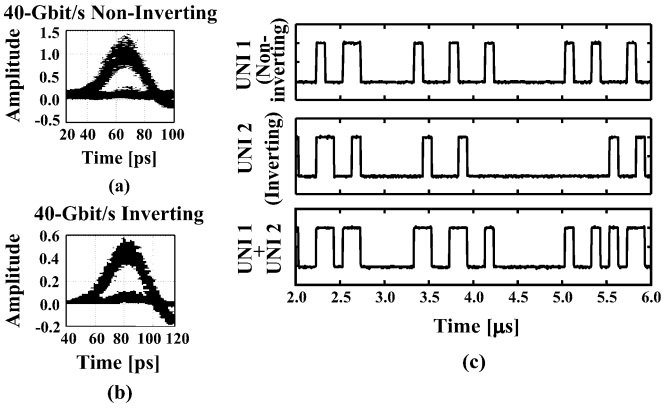

Fig. 4. Eye diagram of the (a) noninverting UNI logic gate and (b) inverting UNI logic gate. The total output (c) of the optical header processor unit performing the logical function $R = E_1 \cdot A_1 + E_2 \cdot \bar{A}_2$.

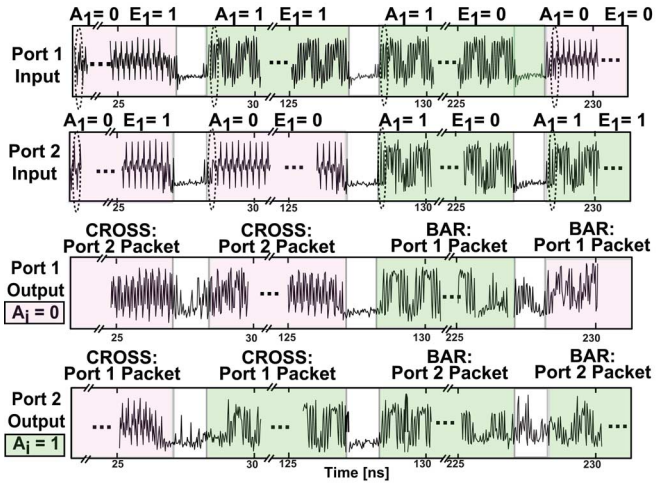

Fig. 5. System demonstration of the all-optical header processing unit. Four 100-ns packets at 40 Gb/s are correctly forwarded through the 2×2 electrooptic spatial switch by the all-optical ultrafast header processor unit. A_i and E_i indicate the address bit and "Empty/Full" bit, respectively, for a packet arriving at Port i of the 2×2 switch. (Color version available online at http://ieeexplore.ieee.org.)

Oscilloscope traces were also taken at the output of the 2×2 electrooptic spatial switch to provide a visual demonstration of the correct operation of the 2×2 spatial switch when driven by the all-optical ultrafast header processor. For this demonstration, two visually distinct 4000-bit 100-ns packets were designed. The first packet uses a "10" repeating pattern and the second packet uses a "11110000" repeating pattern. The "Empty/Full" bit pattern remained the "1001" pattern. Again, the input packet streams at the two ports on the 2×2 electrooptic spatial switch are distinguished by a 100-ns single-packet delay. Variable delays on the address inputs to the UNI logic gates are used to select one bit in the packet as the address bit and ensure a nondegenerate result from the header processing logic. Adjacent packets are separated with a 1.5-ns guard band to allow for the switching time of the 2×2 spatial switch. The output of the 2×2 spatial switch is detected by two 50-GHz photodetectors and displayed on a 40-GSample/s real-time oscilloscope. Four cases are illustrated in Fig. 5: 1) both packets are full and contending; 2) the Port 1 packet is full and desires the cross state while the Port 2 packet is empty; 3) both packets are empty; and 4) the Port 1 packet is empty while the Port 2 packet is full and desires the bar state.

IV. Conclusion

All-optical ultrafast header processing can reduce packet processing delay and congestion in packet routers as network channel data rates increase to 40 Gb/s and beyond. Multipacket processing is necessary for general network topologies. Here, we demonstrate 40-Gb/s all-optical header processing using two UNIs to simultaneously forward two packets through a 2×2 spatial switch. We achieve clear open eye diagrams with a total measured packet error rate of 10^{-6}, achieving low-error-rate forwarding decisions for packet routing. This all-optical header processing design has the potential for subnanosecond processing delays with monolithic integration of the optical logic gates.

References

[1] B. A. Small, A. Shacham, and K. Bergman, "Ultra-low latency optical packet switching node," *IEEE Photon. Technol. Lett.*, vol. 17, no. 7, pp. 1564–1566, Jul. 2005.

[2] D. J. Blumenthal, P. R. Prucnal, and J. R. Sauer, "Photonic packet switches: Architectures and experimental implementations," *Proc. IEEE*, vol. 82, no. 11, pp. 1650–1667, Nov. 1994.

[3] E. Kehayas, G. T. Kanellos, L. Stampoulidis, D. Tsiokos, N. Pleros, G. Guekos, and H. Avramopoulos, "Packet-format and network-traffic transparent optical signal processing," *J. Lightw. Technol.*, vol. 22, no. 11, pp. 2548–2556, Nov. 2004.

[4] M. C. Cardakli, S. Lee, A. E. Willner, V. Grubsky, D. Starodubov, and J. Feinberg, "Reconfigurable optical packet header recognition and routing using time-to-wavelength mapping and tunable fiber Bragg gratings for correlation decoding," *IEEE Photon. Technol. Lett.*, vol. 12, no. 5, pp. 552–554, May 2000.

[5] I. Glesk, J. P. Solokoff, and P. R. Prucnal, "All-optical address recognition and self-routing in a 250 Gbit/s packet-switched network," *Electron. Lett.*, vol. 30, no. 16, pp. 1322–1323, 1994.

[6] D. Cotter, J. K. Lucek, M. Shabeer, K. Smith, D. C. Rogers, D. Nesset, and P. Gunning, "Self-routing of 100 Gbit/s packets using 6 bit 'keyword' address recognition," *Electron. Lett.*, vol. 31, no. 25, pp. 2201–2202, 1995.

[7] S. A. Hamilton and B. S. Robinson, "40-Gb/s all-optical packet synchronization and address comparison for OTDM networks," *IEEE Photon. Technol. Lett.*, vol. 14, no. 2, pp. 209–211, Feb. 2002.

[8] F. Ramos, E. Kehayas, J. M. Martinez, R. Clavero, J. Marti, L. Stampoulidis, D. Tsiokos, H. Avramopoulos, J. Zhang, P. V. Holm-Nielsen, N. Chi, P. Jeppesen, N. Yan, I. T. Monroy, A. M. J. Koonen, M. T. Hill, Y. Liu, H. J. S. Dorren, R. Van Caenegem, D. Colle, M. Pickavet, and B. Riposati, "IST-LASAGNE: Towards all-optical label swapping employing optical logic gates and optical flip-flops," *J. Lightw. Technol.*, vol. 23, no. 10, pp. 2993–3011, Oct. 2005.

[9] S. A. Hamilton and B. S. Robinson, "> 100 Gbit/s time-domain processing techniques for optical packet switching," in *Optical Fiber Communication Conf., 2004 (OFC 2004)*, Feb. 2004, vol. 1, pp. 23–27.

[10] B. S. Robinson, S. A. Hamilton, and E. P. Ippen, "Multiple wavelength demultiplexing using an ultrafast nonlinear interferometer," in *Conf. Lasers and Electro-Optics (CLEO'01)*, 2001, vol. 528.

[11] N. S. Patel, K. L. Hall, and K. A. Rauschenbach, "Interferometric all-optical switches for ultrafast signal processing," *Appl. Opt.*, vol. 37, no. 14, pp. 2831–2842, 1998.